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A SYNCHRONOUS DATA COMPRESSION SYSTEM

by

Joseph S. Calcagno

A Thesis Submitted
in
Partial Fulfillment
of the
Requirements for the Degree of
MASTER OF SCIENCE
in
Electrical Engineering

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PREFACE

A unique sequence of events made the subject of this thesis possible. In June of 1974 my supervisor (at Xerox Corporation) asked me to develop a specification for a general purpose data acquisition system (D.A.S.). This was a low priority task and required about six months of spare time to complete. The D.A.S. system was not continued because of higher priority work. Because of my interest in D.A.S. systems, I continued to develop the system design on my own.

In July of 1975 I transferred to a new department. An engineer in this department was in the process of ordering three chart recorders to be used for a series of experiments. After showing him the advantages of using my D.A.S., he cancelled his order and gave me the go-ahead to build the D.A.S. Since this was not my primary assignment, I got my supervisor's approval to undertake this task on the condition that it would be operational in four months, would be 100% designed, built, and debugged by me, and would not interfere with my primary activities. The D.A.S. was made operational by December 1975, but required many nights and weekends.

I entered the Master's degree program (M.S.E.E.) in the winter quarter of 1975. Professor George A. Brown agreed to be my lead advisor for a thesis on the data acquisition system and the thesis was started in March 1977.

I wish to thank Professor George Brown for his guidance and assistance during the 18 months that I worked on the thesis. I also wish to thank Dr. Swaminathan Madhu who is the Director of Graduate Programs for the College of Engineering at the Rochester Institute of Technology for allowing me to use the D.A.S. as the subject for my thesis.

I wish especially to thank my wife for her support, encouragement, and sacrifice. A special thanks goes to my sister Marge Hodges for typing the thesis. Last but not least are my two children David and Janet, who understood why their father's presence was so scarce during the preparation of this thesis.

ABSTRACT

This thesis discusses in detail the steps required for the design of a general purpose Data Acquisition System (D.A.S.). This D.A.S. is called a Synchronous Data Compression System (S.D.C.S.) because of some special features.

The S.D.C.S. is designed to accept data in analog or digital form. A simple control panel interface is developed, and areas of prime interest such as input/output interface control, analog-to-digital conversion, data compression, and data sampling modes are discussed in detail.

The primary logic type used for the S.D.C.S. is the CMOS type 4000 Series which was developed by R.C.A.

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SYMBOL	
N	Columns per line.
D	Data value.
E	Compare tolerance.
V_D	Analog data value.
V_R	Analog value equal to .075% of full scale.
I_f	LED digit segment current.
V_{cc}	Logic supply voltage of +5 VDC.
P_t	Power dissipation of one LED seven-segment digit.
f	Clock for A/D converter.
T_1	Period of f.
T_2	Total conversion time.
R_f	Feedback resistance.
R_{IN}	Input resistance.
I	Charge current.
I_o	Offset Current
T_D	Time, expressed by a clock-count.

1. Introduction

This thesis describes the design and construction of a general purpose Data Acquisition System (D.A.S.) which can be used to monitor analog and digital data. The development of the D.A.S. is dependent upon existing hardware, and the latest CMOS integrated circuits in the 4000, 4500, and 74C00 families. Other integrated circuit types are used where higher power or switching speeds are required.

The D.A.S. is designed to acquire data in a synchronous manner so that data plots can be more easily obtained automatically. Print-out of data is accomplished in any of four data acquisition modes. The primary (and most useful) mode is the "data compression" mode which is explained in paragraph 5.3. Because of the two important features of synchronous data acquisition and of data compression, this system is described as a Synchronous Data Compression System (S.D.C.S.).

The subject of this thesis has been organized in four parts. The first part (para. 3.1) develops the system specification. The second part (para. 3.2) develops two or more solutions to each sub-system requirement and selects the best solution. The third part (para. 4) develops the primary and secondary system timing, and the fourth part (para. 5) develops each sub-system design.

2. Historical Review

Data acquisition associated with engineering development of components and products has accelerated dramatically since its primitive beginning which essentially started during the early 1900's. Companies such as General Electric, Westinghouse, and RCA were among the pioneers in this field.

Data acquisition requires transducers to convert a physical phenomena of interest into an easily measured electrical signal. Transducers developed in step with the necessity to measure newly discovered phenomena. It is not surpising to note, therefore, that long before there was any such thing as a steady electric current, that is before 1800, attempts were being made to estimate the strength of a magnet and the value of a static potential.

Today there are literally hundreds of transducers used for measuring temperature, force, time, pressure, flow, velocity, acceleration, humidity, viscosity, and literally hundreds of other physical measurements. Data acquisition, evaluation, reduction, and presentation has become more sophisticated as the data acquisition systems evolved from the vacuum tube, to the transducer, then to the integrated circuit. The most sophisticated systems employ computers and mass data storage.

The microprocessor is rapidly replacing the medium size data acquisition system in the laboratory. Many companies are introducing microprocessor-based data acquisition systems. Tailored data acquisition systems can be easily built by combining a microcomputer board, say from Intel Corp.,

Motorola, Digital Equipment, Pro-Log or Zilog, with an analog I/O board from companies such as Burr-Brown, Analog Devices, Datel and Analogic. The addition of transducers, control panel interface, storage - such as disc or magnetic tape, and a printout device will provide a full-fledged data acquisition system.

Many companies are introducing microprocessor-based data acquisition systems which require only the addition of transducers and an output device which accepts ASCII coded data.

3. Data Acquisition System Development

A data acquisition system has little value if it does not satisfy the requirements of the user. In this case, the user is testing an electro-mechanical piece of equipment and is monitoring analog and digital forms of data from it. He is primarily interested in instantaneous printout of all data for visual examination.

3.1 Development of the System Specification

The Synchronous Data Compression System (S.D.C.S.) requirements are as follows:

3.1.1 Data Input

The system shall be designed to accept analog and digital data. The analog signal conditioning electronics shall be mounted on a printed circuit board and will be located in the bottom-half of the S.D.C.S. chassis. Interface requirements for digital data channels can also be mounted on an input printed circuit board.

3.1.2 Data Output

A line printer shall be used to obtain a printout of the test data. The control panel can also be used to monitor a selected data channel.

3.1.3 Print Format

Time and all data channels shall be printed in one line. The specific printout format will be developed later.

3.1.4 Data Sample and Print Rate

All data channels will be sampled at a rate which shall not exceed the maximum print rate. The maximum print rate is dependent upon the line printer which will be selected later.

3.1.5 Data Compression

In this mode of operation, data will be printed only if one (or more) data channel(s) exceeds a specified percentage of change with respect to the last printed data value(s). Data compression is explained in detail in Section 3.2.1, Page 21 thru 32.

3.1.6 Selectable Data Print Rate

In this mode of operation, time and all data channels can be printed in one line at any one of the following fixed rates:

a. One line per second.

b. One line per 10 seconds.

c. One line per minute.

d. One line per 10 minutes.

The S.D.C.S. can operate in the Data Compression mode, in the fixed rate mode, or in both modes simultaneously.

3.1.7 Manual Print Request

One line of data shall be printed when the PRINT REQUEST switch is activated.

3.1.8 Automatic Print

One line of data shall be printed when a digital channel has valid data. This can occur at the maximum print rate which will be determined later.

3.1.9 Control Panel Features

a. Channel Monitor Capability

The control panel shall contain LED digits to display the selected data channel number, data compression tolerance, and data value, including sign. The monitor functions shall operate as follows:

1. Channel Number Selection and Display

Two touch buttons are available for incrementing or decrementing the channel number at a rate of two counts per second. Channel ø is used to display the real-time clock. Channel number 1 thru N shall monitor data channels 1 thru N respectively. Channels N+1, N+2, and N+3 shall contain reference voltages for calibration of the A/D converter.

2. Channel Data Display

The selected channel data value and polarity shall be displayed on L.E.D. digits. Analog channels are updated every 0.5 seconds. When a digital channel is selected, the display will hold the last valid digital value indefinitely.

3. Data Channel Tolerance Display

The tolerance of the selected data channel will be displayed on two L.E.D. digits. Two touch buttons are available for incrementing or decrementing the tolerance of the selected channel at a rate of two percentage counts per second. The tolerance range for each channel is 1 thru 15 percent and 99 (or OFF) percent. When power is turned on, all stored data tolerances shall be initialized to 99 percent.

b. Data Compression Sample Rate

At this time an arbitrary number of four switches shall be used for selecting one of our data compression rates. The data compression rates will be selected when the maximum print rate is determined. The four switches shall be momentary and made to function as interlock switches. An L.E.D. lamp shall be located above each switch for the purpose of indicating the selected data compression rate. When power is turned on, all data compression rate indicators will be turned off.

c. Fixed Data Sample Rate

A touch-button switch is available for selection of each of the data sample rates. The four required switches will be momentary and made to function as

interlock switches. An L.E.D. lamp shall be located above each switch for the purpose of indicating the selected data sample rate. The S.D.C.S. shall be made to operate in the data compression mode only, in the data sample rate mode only, or in both modes simultaneously. When power is turned on, all data rate indicators will be off.

d. Data Request

One line of data shall be printed when the DATA REQUEST switch is activated. An L.E.D. lamp shall be located above this switch and shall illuminate when the switch is activated.

e. Control Panel Lock Switch

A LOCK switch shall be used to prevent accidental activation of the Data Compression and Data Sample Rate switches. An L.E.D. lamp shall be located above the LOCK switch and shall illuminate when the LOCK switch is activated. When power is turned on, the LOCK switch shall be activated.

f. Printer ON/OFF Switches

Activation of the PRINTER ON switch shall enable data transfer to the line printer. Activation of

the PRINTER OFF switch shall inhibit data transfer to the line printer. An L.E.D. lamp shall be located above each switch to indicate which switch is activated. When power is turned on, the PRINTER OFF L.E.D. lamp shall be illuminated.

g. Control Panel Switches

The operator shall be allowed to change the channel number, data tolerance memory, data compression or data sample rates while the printer is on (or off) without causing irregular or false printout. Activation of the PRINTER OFF switch shall not cause false or partial printout.

3.1.10 Common I/O Interface

The I/O interface to the analog and digital printed circuit boards shall be designed to allow any printed circuit board type to plug into any connector location.

3.1.11 Data Channel Inputs

The following factors will determine the number of data channels:

a. Selection of a standard (commonly used) type of line printer.

b. The requirement to print time and all data channels in one line.

c. The number of characters required per data channel. This is dependent upon the following factors:

   1. Data resolution required.

   2. Requirement of polarity indication and decimal point.

   3. Separation of data channels by at least one letter space.

   4. Special characters, if required.

d. The type of hardware which is available for data channel plug-in modules.

e. The number of data channels per plug-in module.

3.1.12 Analog Data Conversion Accuracy

The primary aim of the Synchronous Data Compression System (S.D.C.S.) is to monitor those types of systems where high accuracies are not required. Using present-day components, a data system with an overall accuracy of 0.1 to .15 percent of full scale should be considered. This includes signal conditioning, multiplexing, and analog-

to-digital (A/D) conversion.

Polarity is a desirable feature and should, therefore, be included. Measurements such as ± D.C. volts, temperature, deceleration and differential pressure are only a few examples of bipolar measurements.

Resolution and polarity requirements dictate that the A/D converter must have an accuracy of ±.05 percent, ± 1 bit, and analog conditioning would also have a ±.05 percent accuracy. The A/D converter must then have at least an 11 bit binary or a 3-1/2 digit BCD resolution. In either case, printout will be a 3-1/2 digit signed value with decimal point. Considering that data printout should have at least one letter space between data channels, a total of seven columns is required per data channel. The logic design can be simplified by using the same number of columns for time and data. The equation for the number of data channels (X) which can be printed in one line of N columns is then:

$7 (X + 1) = N$

or: $X = (N/7) - 1$

N = 80 for the standard 80 column printer and:

$X = (80/7) - 1 = 10.43 = 10$ data channels.

For a standard 132 column printer:

$X = (132/7) - 1 = 17.86 = 17$ data channels

Hardware is another consideration. Vector Corporation makes a 19 inch wide card cage which can hold eight 2.0 inch wide card modules or ten 1.6 inch wide card modules. A card module is a metal box which houses a P.C. board and can be placed into a Vector card cage. The P.C. board has an edge connector which extends beyond the back side of the card module and which inserts into a mating connector on the back of the card cage. On the assumption that Vector's standard 9.6 inch long by 4.5 inch wide component card can hold the required electronics for the signal conditioning of two data channels, the 1.6 inch, ten module cage looks most attractive. This arrangement allows a maximum of 20 data channels vs. 16 for the 2.0 inch, eight module cage.

Previous calculations have shown that only 17 data channels can be printed in one line for a 132 column printer. This number can be increased if we allow the decimal point to be replaced by another symbol when the most significant digit of the 3-1/2 digit value is a one, i.e. when the data value is 1,000 or greater. This symbol will indicate that a "1" must be inserted immediately to the right of the plus (or minus) sign. Selection of the "$" symbol will be made because it cannot be mistaken for any of the other

characteristics to be printed and also because it has the same ASCII upper - MSB code (excluding Bit 8).

This numbering technique limits the data value to 1999, which corresponds to the maximum value of a 3-1/2 digit number. Full scale is then defined as the maximum 3-1/2 digit value of 1999.

The following are examples of the actual number and the printed number:

ACTUAL NO.	PRINTED NO.
+12.68	+2$68
-1024.	-024$
+1.997	+$997
-62.4	-62.4

This format allows time and data values to be printed in only six columns each. A 132 column printer can then print the following number of channels:

Let X = No. of CHANNELS
Let N = 132 columns
Then 6 (X+1) = N = 132
$\therefore$ X = (132/6) - 1 = 21 data channels

A line of printed data will then consist of time and twenty data channels. An example of a partial line of printout showing time (in seconds) and three data channels is shown below.

(SP) 431.6	(SP) + 26.4	(SP) - 9.44	(SP) - 1$27
TIME (IN SEC.)	DATA	DATA	DATA

Note: (SP) = Letter Space

To obtain a time printout to a tenth of a second requires a printer which is capable of printing at a rate of at least 10 lines per second. Versatec is a company which manufactures line printers and was recently acquired by Xerox Corporation. Versatec is then the logical company to select for the purchase of a line printer. Table 3.1 is the Matrix Model Selection Chart for the Versatec printer line. No 132 column printers are available at the 10 line per second (600 LPM) speed. The only choice is the Model LP-D1175 which is a 1000 LPM (16-2/3 lines per second), 132 column printer. This unit has a one-line buffer which can be loaded at a maximum rate of one million characters (ASCII code) per second. This buffer can be used to store time and data at the maximum rate of 10 lines per second. After each line is stored the decision to print the line buffer or clear it can be made. The data buffer can be cleared with a CLEAR signal or printed with a carriage return (CR) ASCII character or the transmission of 132 characters. When the print mode is initiated the line printer sends a BUSY signal to the S.D.C.S. which lasts for 60 milli-seconds. Since the line buffer cannot receive new data during the BUSY time, all data must then be transferred

TABLE 3.1

MATRIX MODEL SELECTION CHART

PRINT LPM	11 x 8.5 INCH PAPER		
300		LP-D1616	
500	LP-D1150		LP-D1250
600			
1000	LP-D1175		
COLUMNS PER LINE	132	100	132

during the remainder of the 100 millisecond per line period (40 milliseconds). If only 20 channels of data were printed in one line, then each channel could be processed and transmitted every 2 milliseconds. Each line of data also requires a printout of time. If time is transmitted at the same rate as data, then 1.9 milliseconds is the maximum allowable data process time per channel. It is very desirable to use a process time which is an even multiple of 10 because each data channel is processed at a rate of 10 times per second, or every 100 milliseconds. A master timing system which uses BCD counters is ideal in this system. The logical time selection for processing each channel is then 1.0 millisecond.

3.2 Choosing Between Various Sub-System Design Approaches

The Synchronous Data Compression System (S.D.C.S.) design will be developed using the Top-Down design[1] technique. Top-Down design starts a solution at the highest level, or most global view of a problem, and proceeds downward to levels of increased detail only after the analysis and decision process has been completed at higher levels.

The first level block diagram of the S.D.C.S. is shown in Fig. 3.1. At this level, only the primary elements are shown, and include the control panel, data input conditioners, system control, and the line printer. The next level of complexity is shown in Fig. 3.2. This level shows the system elements required for interface to the control panel, data signal conditioning section, and the line printer. The requirement for system timing and control is shown here, but will not be developed until the final design approach to all sub-system functions is determined.

The next step (Fig. 3.3) in the design is to define all the functional elements and their logical interconnections. This design stage is still conceptual, without considerations of implementation. Figure 3.3 shows all the sub-system components of the S.D.C.S. The next task involved selection of the optimum digital or analog design for each sub-system.

1. Matthew L. Fichtenbaum
"Top-Down Design Streamlines Digital System Projects,"
Computer Design, Sept. 1976, pp. 91-96.

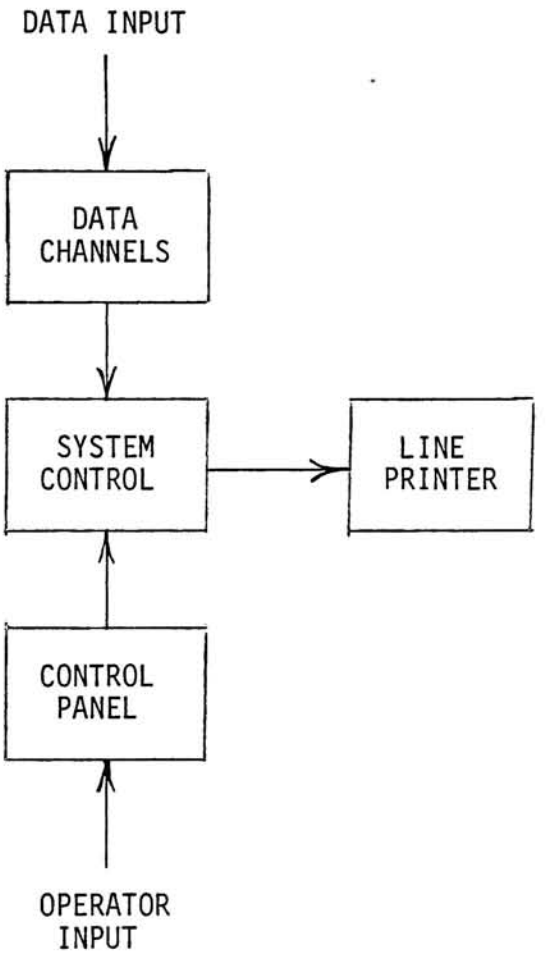


Fig. 3.1 FIRST-LEVEL BLOCK DIAGRAM OF THE S.D.C.S.

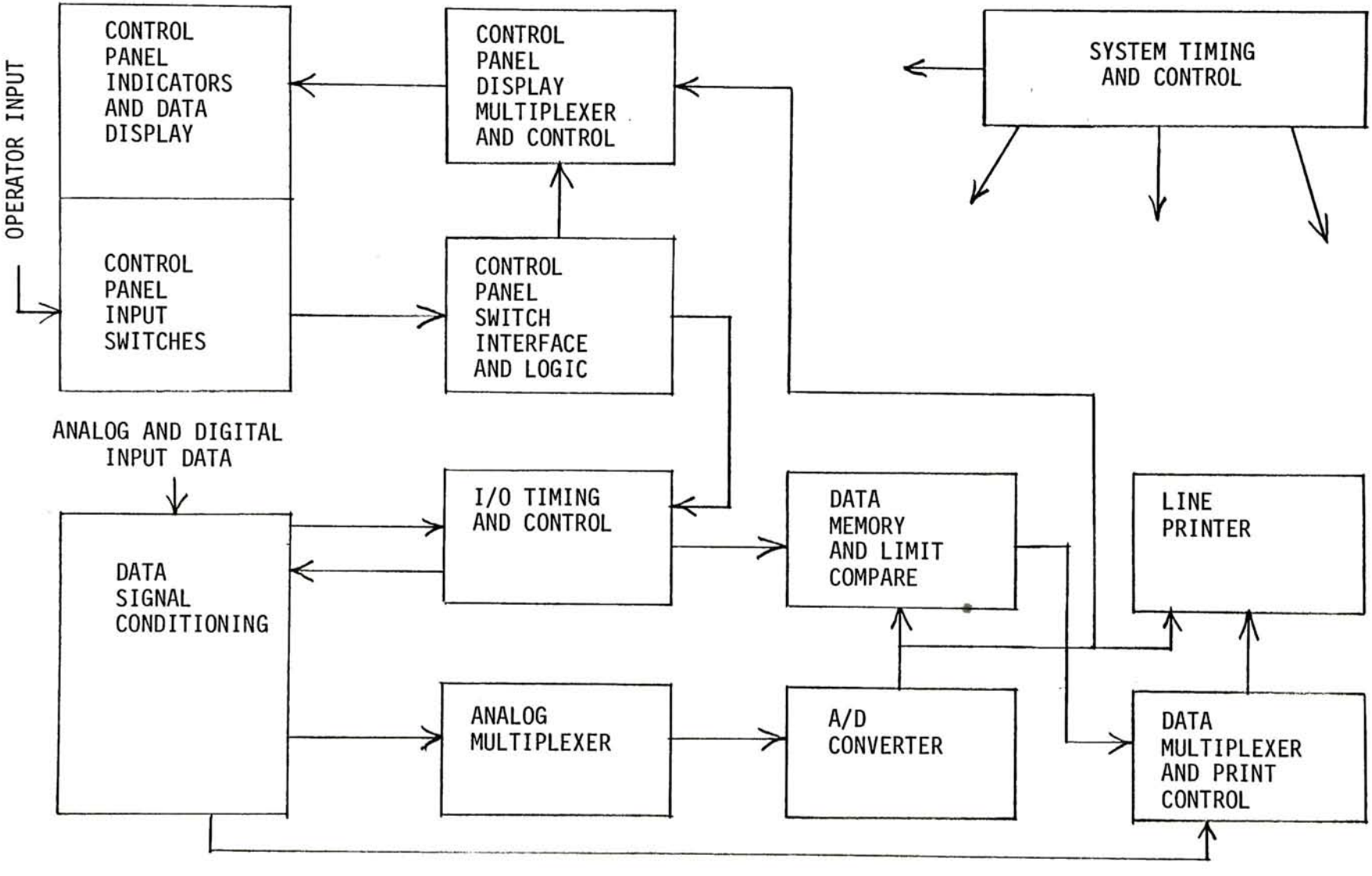


FIGURE 3.2 SECOND-LEVEL BLOCK DIAGRAM OF THE S.D.C.S.

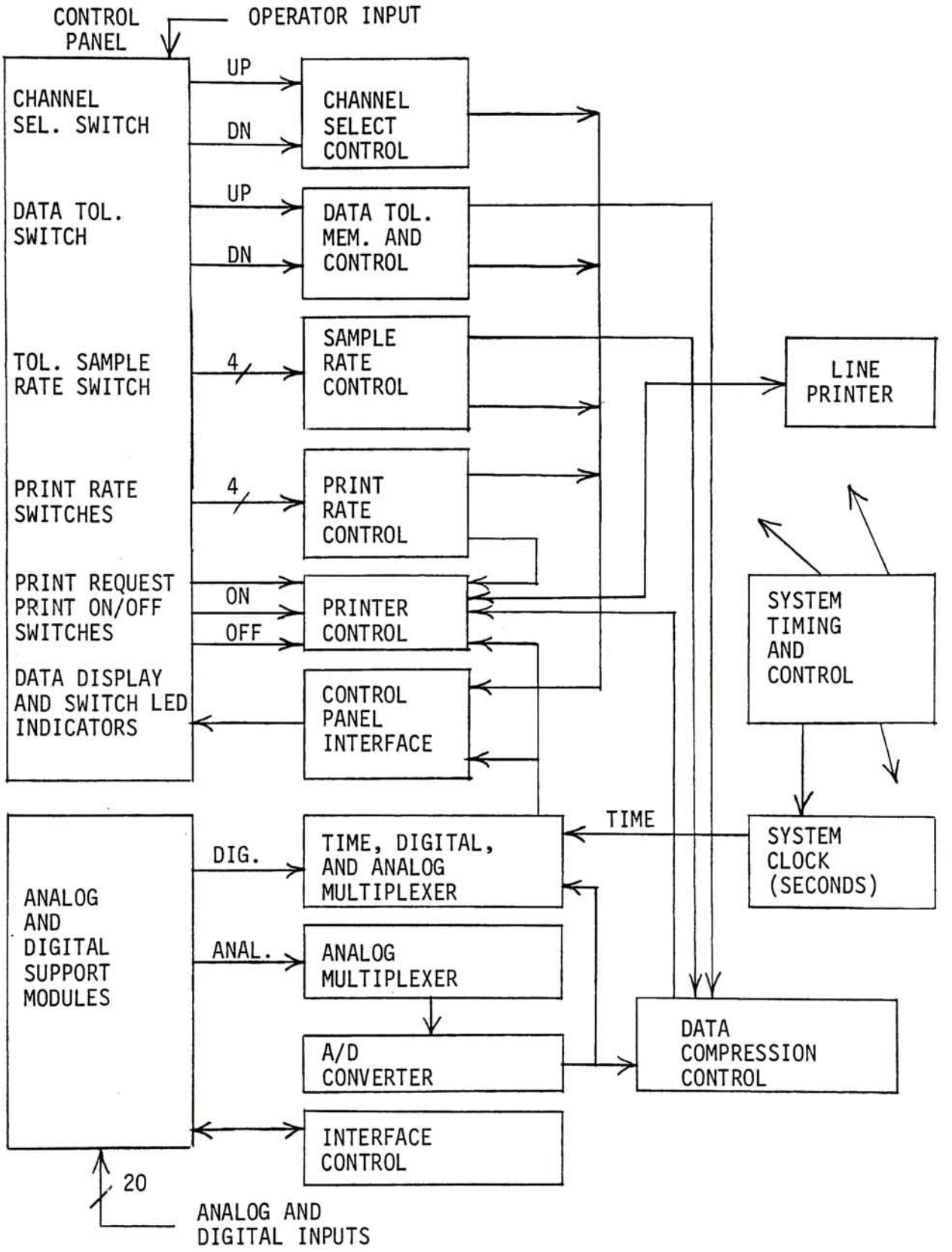


FIGURE 3.3 - SUB-SYSTEM COMPONENTS OF THE S.D.C.S.

3.2.1 Selection of the Data Compression Control Sub-System

This sub-system is selected first because it is the most interdependent of all sub-systems. The solution to this sub-system will require a specific partial solution to inter-related sub-systems as will be shown.

At this point, a description of the data compression function is in order. Data compression is simply a method of reducing the amount of data to be considered (printed) for evaluation. If a number of data channels are monitored, it is important to print all data channels every time one or more data channels changes by a "Specific amount." This "specified amount" can be defined as any of the following:

a. A fixed amount such as $\pm$ 2°C, $\pm$ .3VDC, $\pm$ .27 oz. -in., etc.
b. A percentage of the last value which caused printout.
c. A fixed upper and lower value.
d. A limited number of fixed upper and lower values.
e. Any combination of para. a. thru para. e.

The most acceptable method of data compression would be one in which a data channel would cause a printout each time it changed by a specific amount. This specification would eliminate the choices of para. c. and d. Para. d. could be used, but would become impractical if a great number of fixed points were needed.

The data compression technique listed in para. a. looks good at first, but has disadvantages because of the lower and upper range considerations. If an increment equal to one percent of full scale (1999) is chosen, then data at 5 percent of full scale would have to change by 20 percent to go from 5 to 6 percent of full scale. Yet, when data changes from 50 to 51 percent of full scale, it has only increased by 2 percent of full scale. Para. b. solves this problem by requiring that the data change by a fixed percentage of the last value it had which caused printout. Figure 3.4 illustrates this.

Note that full scale is equal to the maximum number of digital counts from the A/D converter. No change can be less than one count from the A/D converter. Full scale has been defined as a 3-1/2 digit number, or 1999 counts.

Assume that data channel 1 has a tolerance of 10 percent. If a value of 40 counts (point A) caused printout then channel 1 cannot cause printout again until it changed by 10 percent, or four counts. When channel 1 finally reaches a 10 percent limit, printout occurs and a new 10 percent window is created (see Figure 3.4).

The method described in para. b. looks very good, but a problem can exist on the lower end of the data range. As an example, assume that a 5 percent change is selected for channel 1 and it is presently at a count (value) of 9. If the value of the data channel decreases, a printout will

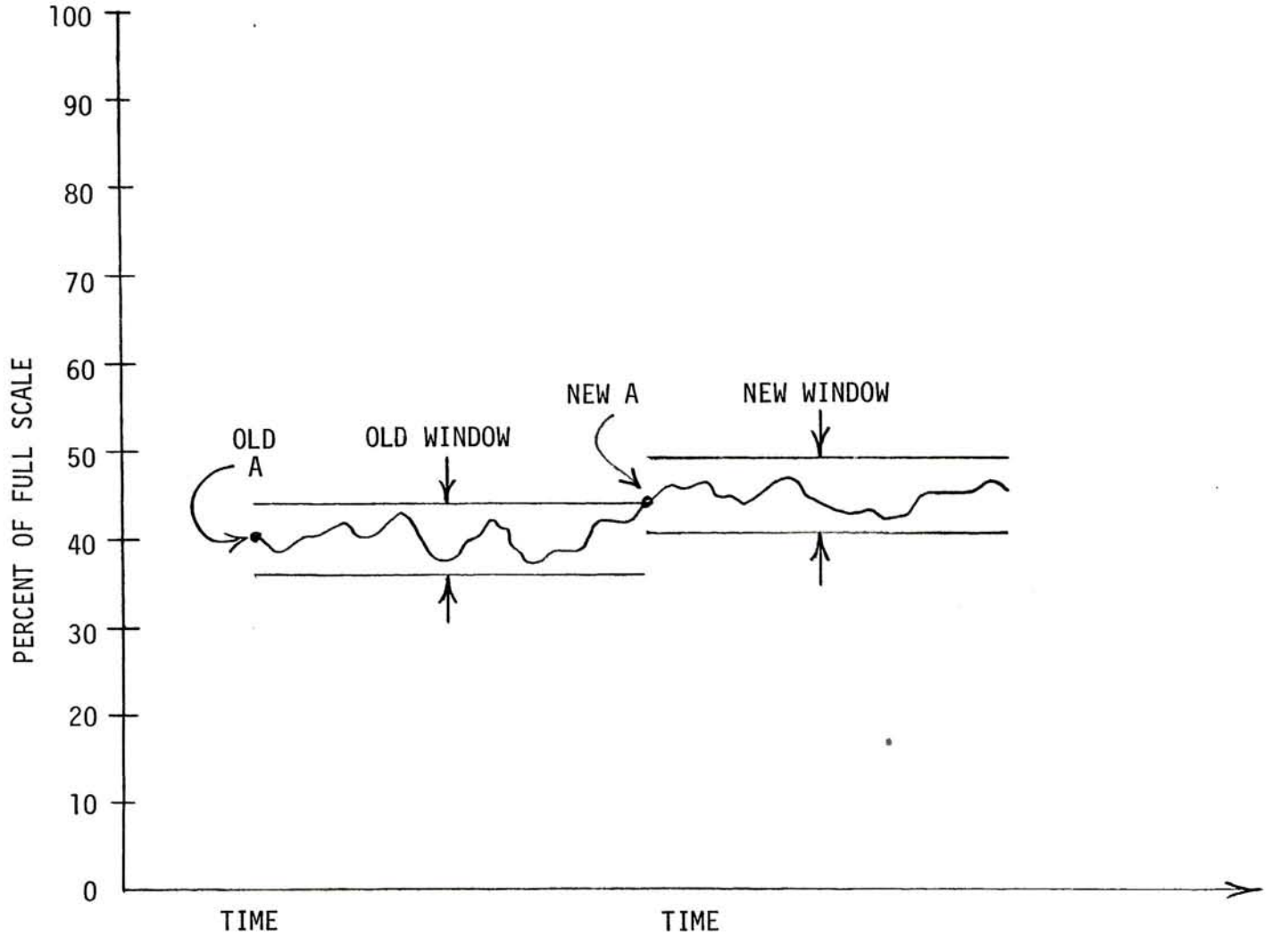


Figure 3.4 DATA TOLERANCE WINDOW EXAMPLE.

occur each time a change of one count occurs. This can be a very undesirable feature. A solution to this problem can be to define the data change as a combination of variables as indicated in para. e. The following combination of variables may be chosen to initiate printout:

- A percentage (of the data value) change.
- A change of at least two counts (from the A/D conversion).
- An absolute data value of at least 15 counts (from the A/D conversion).

This combination of requirements is a very effective compromise of all the stated options, and will therefore be used.

The data compression system now has a defined "WINDOW" in which data may change without causing printout. This "WINDOW" is proportional to the data value (percentage of data), yet has a minimum value ($\pm$ 2 counts) and is only active when the absolute data value is greater than a specified value (15 counts).

As an example, if channel 10 has a percentage voltage of X and printout last occurred at value D, then the new window is:

$D \pm (XD + 2)$

where $D > 15$ counts

A sub-system solution to data compression design can involve any combination of analog and digital solutions. An attempt will be made to solve each function using analog and/or digital solutions.

The requirement for the digital data value to change by at least two counts is then an absolute necessity because an A/D converter is required, and A/D converters always have a minimum conversion accuracy of at least $\pm$ .5 LSB. A typical A/D of modest cost has a total accuracy of $\pm$ .05 percent (of full scale) $\pm$ .5 LSB. For a 3-1/2 digit A/D converter, this translates to an accuracy of $\pm$ 1.5 LSB. Now that this part of the data compression sub-system is defined, we can now consider solutions for the remainder of this sub-system.

A system which favors analog solutions is shown in Figure 3.5. The only function which dictates the use of a digital solution is the memory for the digital data and delta (Δ) data values. The closest analog solution to data storage is a sample/hold circuit. This is impossible to implement because data may need to be stored for several hours.

Because the A/D converter must be used for the digital storage, the next question to be asked is whether to select a dual slope or a successive approximation A/D converter. Present day technology dictates that a dual slope approach

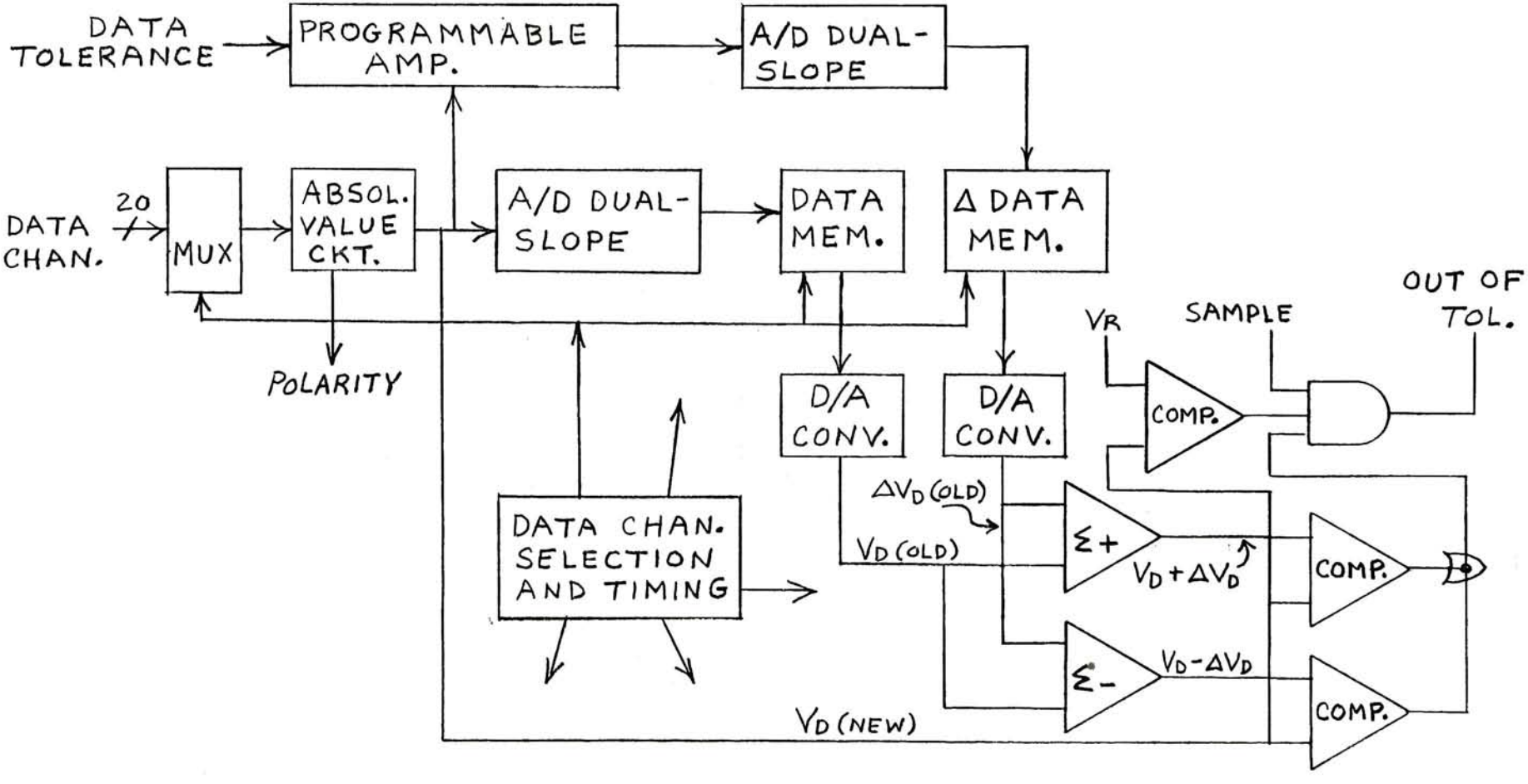


Figure 3.5 Data Compression with a Programmable Amplifier

gives the most accuracy per dollar provided that the conversion speed requirement can be obtained. Another advantage to the dual slope A/D converter is its inherent noise immunity due to the effective integration of the data signal. This is a well-known feature and will not be discussed.

Figure 3.5 shows two A/D converters. One is used to convert the analog value, while the second A/D converter is used to convert a fractional value of the data which is equal to the desired data tolerance. This method has the disadvantages of complex circuitry and inherent conversion errors which exist in the programmable amplifier and the additional A/D converter.

Figure 3.6 shows a better solution for obtaining the data tolerance value. This is a digital solution which requires a BCD Rate Multiplier, an input pulse train from the A/D converter which is equal to the conversion value, and an output counter. The detailed solution for obtaining the data tolerance value will be shown in section 5.3.

The analog solution (Figure 3.6) introduces errors in each D/A conversion (at least $\pm$ .05 percent full scale, $\pm$ .5 LSB), each amplifier ($\pm$ .1 percent linearity), and in each comparator ($\pm$ .02 percent, long term).

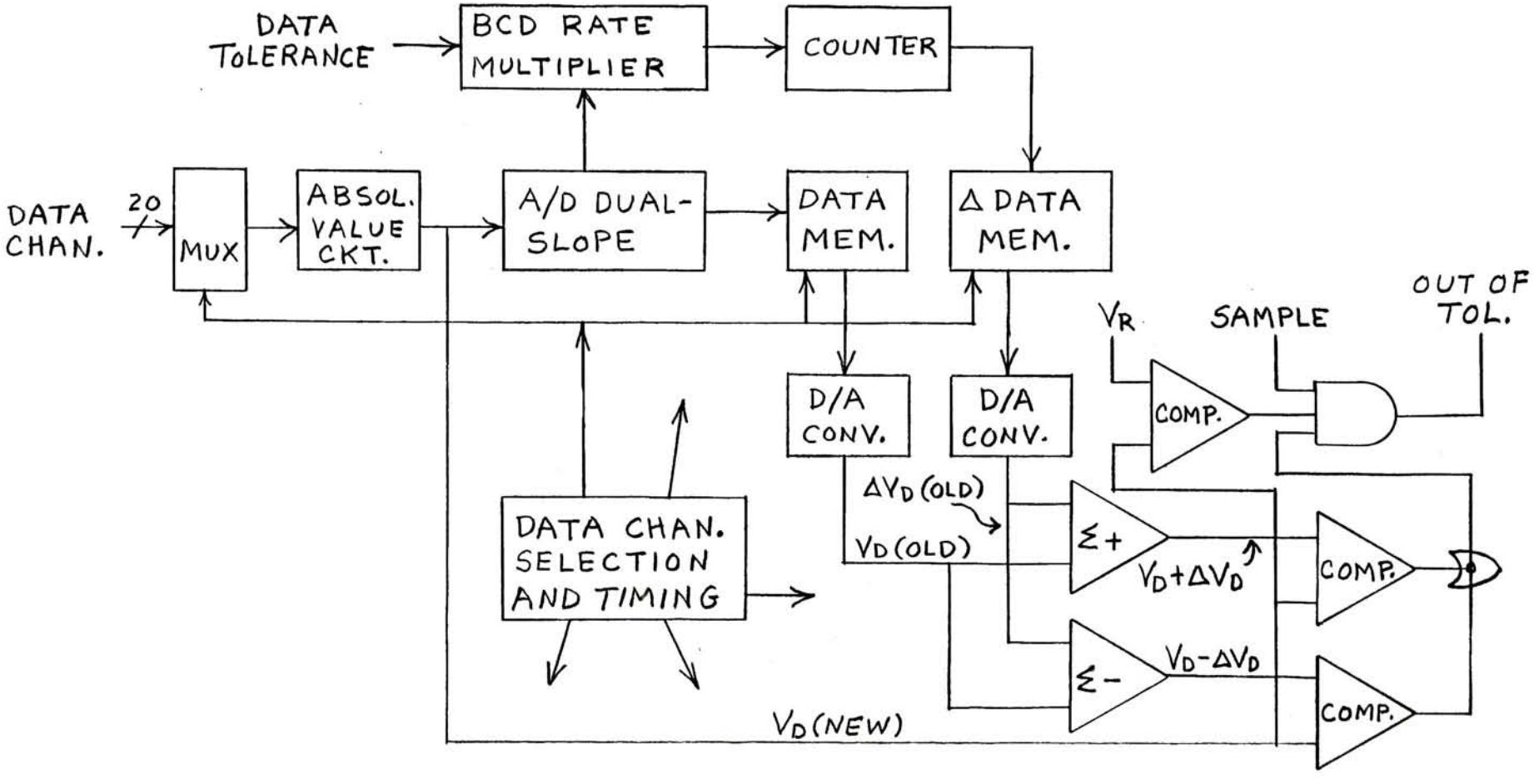


Figure 3.6 Data Compression with a BCD Rate Multiplier

Worst case caluculation of the compare tolerance, E, is then:

$E = 2\ [(.05 + .1 + .02)\% \pm .5\ LSB]$

$= 2\ (.17\% + .5\ LSB) = .34$ percent full scale $\pm$ 1 LSB

This error is tolerable. The only shortcoming to this approach is that there is no noise immunity for the new data input to the comparators, and each comparator would require an offset to widen the compare window by 2 LSB's as defined earlier.

The compare inhibit signal (Figure 3.6) is true as long as new data [V_D (NEW)] is less than V_R. The value of V_R is set to .75 percent of the full scale analog voltage. This circuit satisfies the requirement that printout shall not be initiated when the absolute value of data is equal to or less than 15 counts, or .75 percent of full scale.

One possible modification to the sub-system in Figure 3.6 is a substitution of one D/A converter and the analog ADD/SUBTRACT functions with a digital solution. Figure 3.7 shows one possible solution. The ADD/SUB LOGIC function eliminates any non-linearities which existed when two D/A's were used, and also eliminated the ADD/SUBTRACT amplifiers and their inherent errors.

At this point, one can see that the next possible modification to the Data Compression Sub-System would involve a 100 percent digital solution. Figure 3.8 shows a 100 percent digital solution to the Data Compression Sub-System.

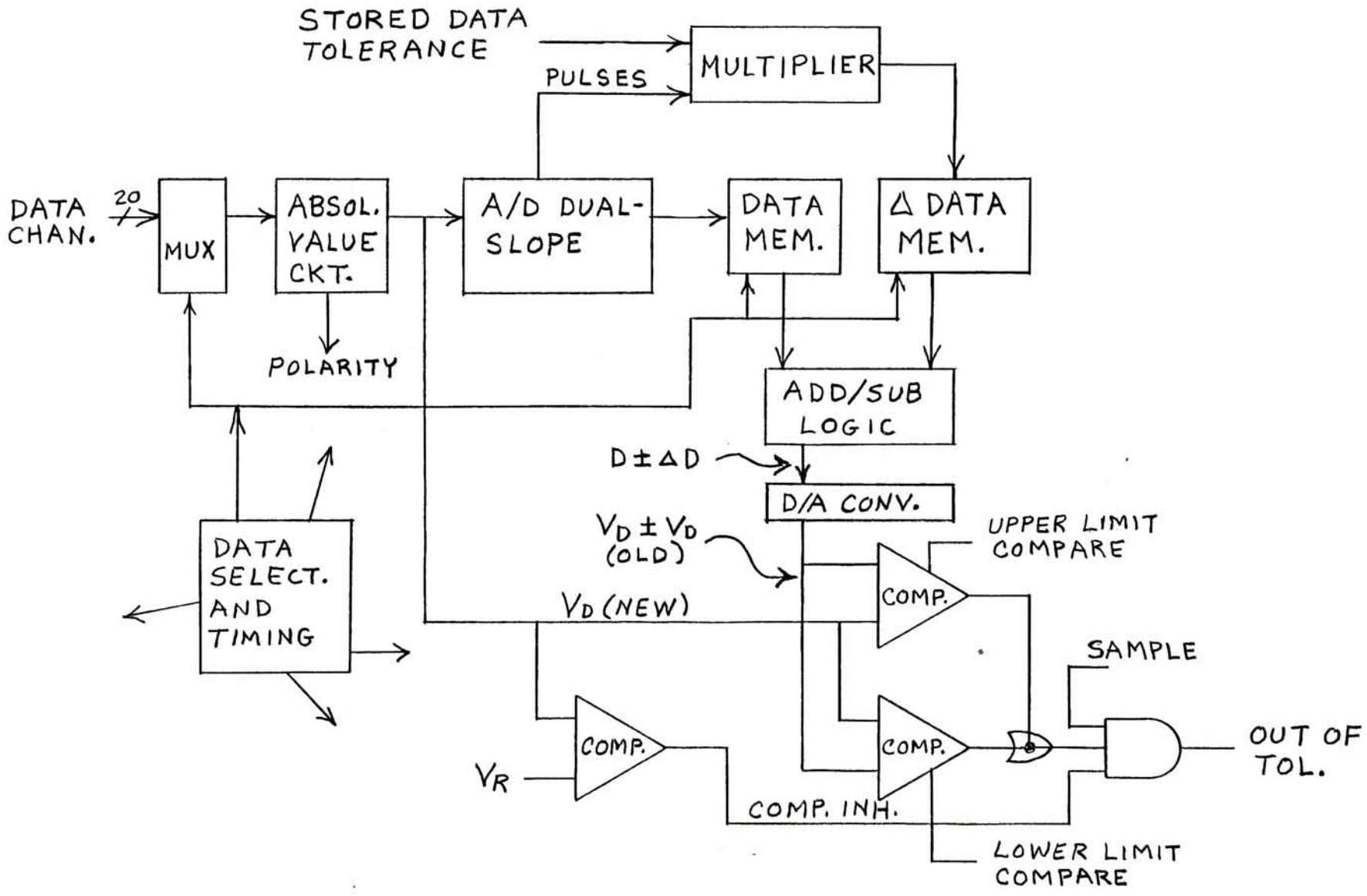


Figure 3.7 Data Compression Using Time-Shared D/A, Add/Sub Logic, and Comparators

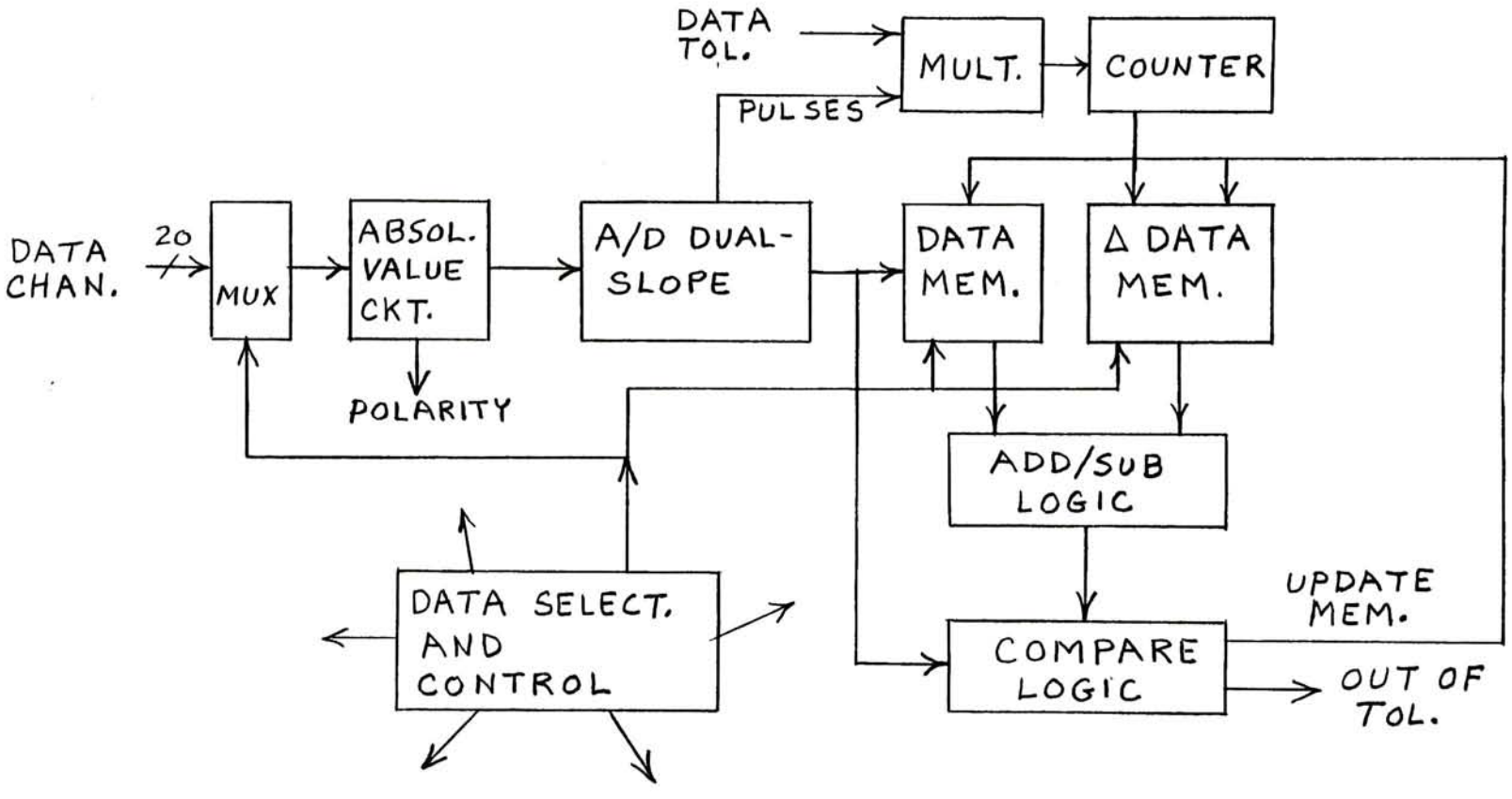


Figure 3.8 Data Compression with an All-Digital Solution

The ADD/SUBTRACT and COMPARE logic functions can be designed using a serial or parallel method. Whichever method is used, both functions will be accomplished using binary coded data because I.C. manufacturers have favored a binary solution for the ADD/SUBTRACT function. The serial solution is attractive because less IC's are required for the ADD/SUBTRACT and COMPARE functions, and much less wiring is required to perform the arithmetic functions.

3.2.2 Selection of the Control Panel Interface Sub-System

a. Selection of Control Switches

The control panel is the operator interface to the S.D.C.S. For this reason its operation and data display must be easily understood. Figure 3.3 shows the various operator input controls and the feedback control of the switch indicators and data display.

The control panel layout is shown in Figure 3.9. The operator can increment or decrement the channel number and channel tolerance to the desired selection, with the data value of the selected channel displayed with a 3-1/2 digit plus polarity display. The switches and indicators for Data Compression Sample Rate, Fixed Data Sample Rate, Data Request, Control Panel Lock, and Printer ON/OFF are on the right side of the Control Panel.

The input controls can be mechanical switches, capacitive touch plate switches, Hall effect switches, conductive touch switches, etc. Since CMOS logic is the primary I.C. type selected for the S.D.C.S., conductive touch switches will be used to take advantage of the high input impedance of CMOS.

b. Selection of the Data Display Interface

The data display interface is shown in Figure 3.10 (a). The data display includes data channel number selection (two digits), data tolerance selection (two digits), and a signed 3-1/2 digit display as shown on the left side of the Control Panel. A method must be selected for transferring this data (eight digits) from the main logic to the eight L.E.D. digits which are located on the control panel display board.

(2) The Engineering Staff of Texas Instruments, Inc., The Optoelectronics Data Book, pp. 293-296.

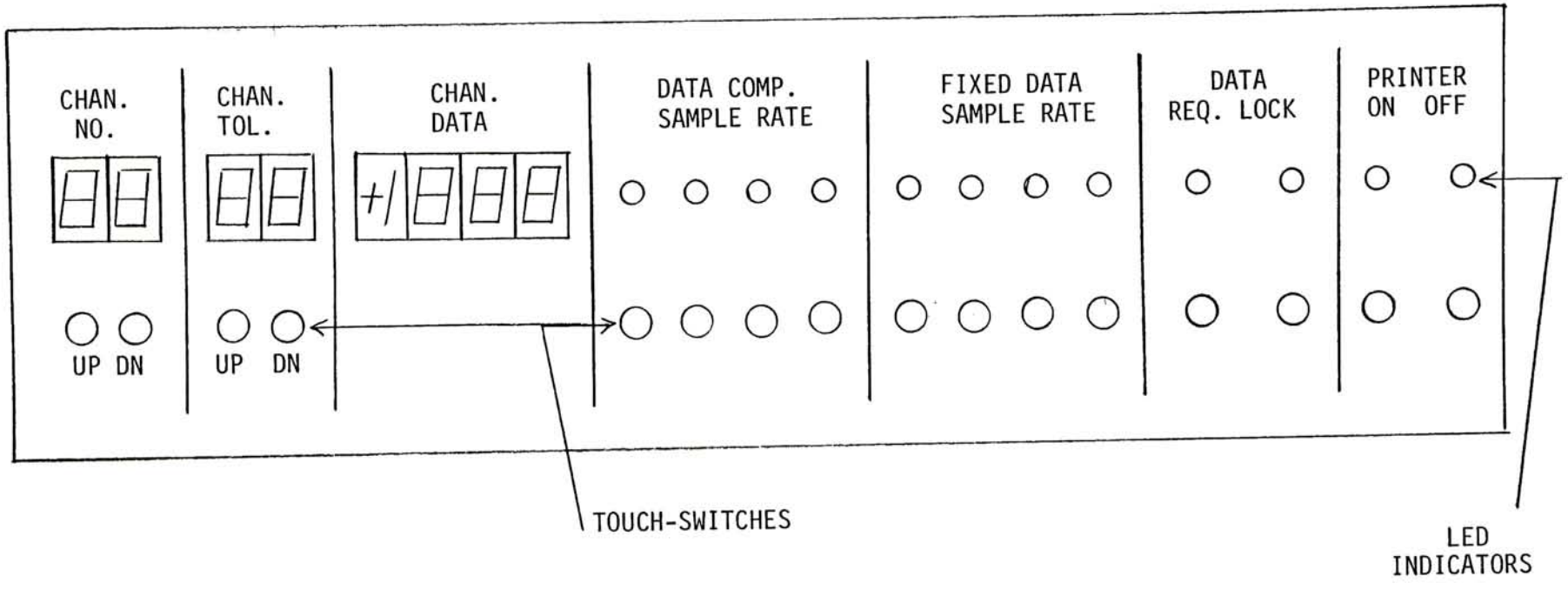


FIGURE 3.9 CONTROL PANEL LAYOUT

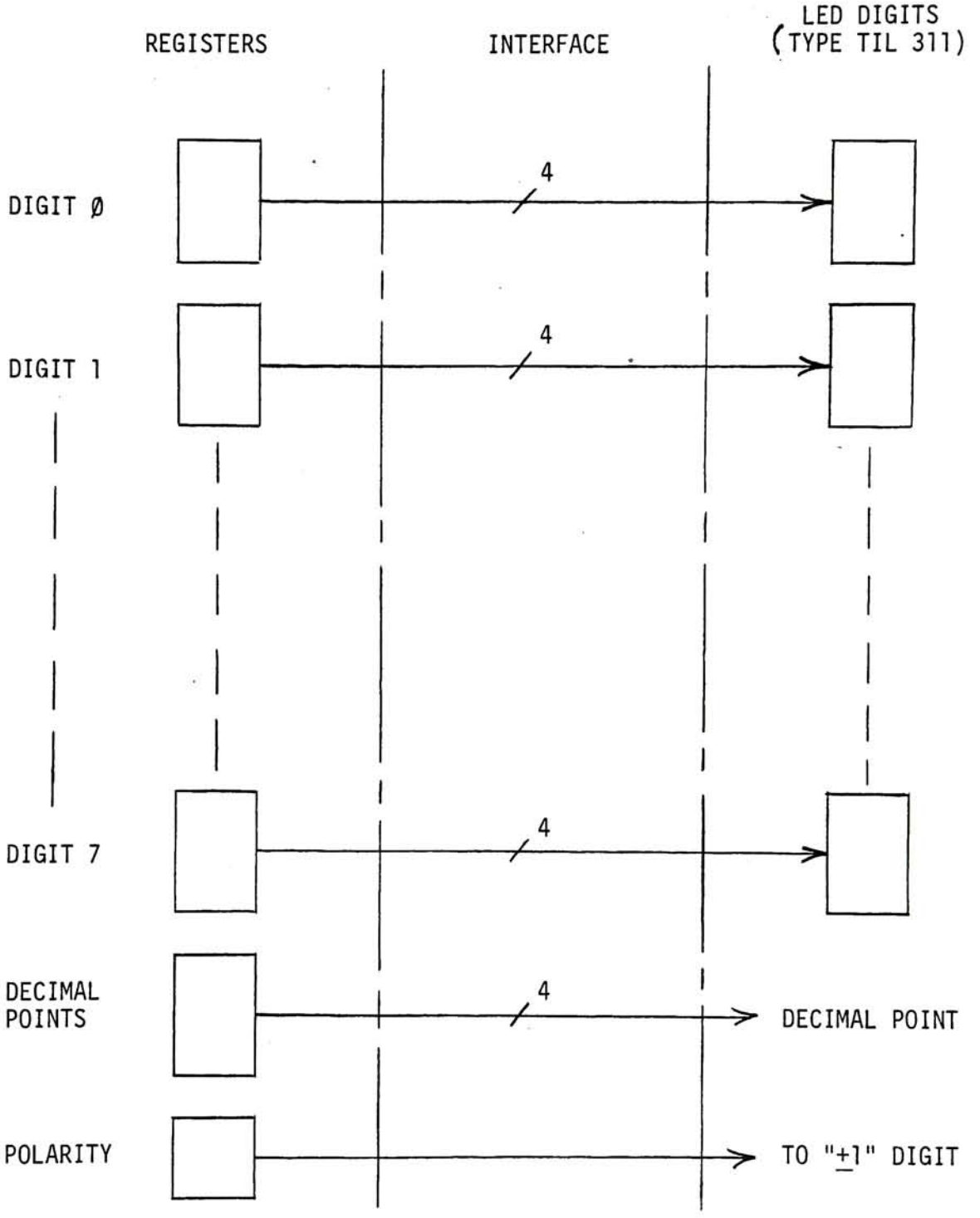


FIGURE 3.10 (a) MAXIMUM-WIRE INTERFACE TO L.E.D. DISPLAY

A brute-force method is shown in Figure 3.10(a). The L.E.D. digits can be Texas Instruments type TIL 311[2] hexidecimal display with logic. The TIL 311 is a 14-pin dual-in-line I.C. which presently has a 100 piece cost of $6.50 each. The I.C. contains a four-bit latch, BDC to 7-segment decoder, 7 constant-current drivers, and the 7-segment L.E.D. display.

The advantages of this design are: 1) a low P.C. board real-estate requirement, 2) low assembly cost, 3) easy to troubleshoot. The disadvantages are: 1) high cost, 2) 37 interface wires required, 3) high power dissipation of 525 milliwatts per I.C. (nominal), 4) the "$\pm$ 1" digit is not available in this series and must be separately driven with discrete components, 5) the character height of .27 inches limits the viewing distance to 10 feet.

This design can be improved by replacing the TIL 311 display by the Type MAN 4610 display[3] which is manufactured by Monsanto. This L.E.D. display has a character height of .4 inches and a 40 percent higher luminous efficiency than the TIL 311 for a segment current of five milliamperes. Each L.E.D. display requires a SN74LS47 driver and seven current limiting resistors. The SN74LS47, MAN4610, and seven resistors cost approximately $5.00 and has a total (typical)

(3) Monsanto, 1977 Solid State Optoelectronics, pp. 93-96.

power dissipation of 210 milliwatts. Disadvantages of this approach are: more P.C. board real estate and higher assembly cost than the TIL 311 design.

Multiplexing is an alternative design approach. With this method only one BCD to seven segment decoder driver SN7446A and seven resistors are required to drive all eight L.E.D. displays. The interface wiring is also reduced to 12 signals, which include four separate decimal point signals for the 3-1/2 digit data display. The disadvantage to this approach is the requirement of multiplexing logic [see Figure 3.10(b)], and the addition of digit drivers.

According to the manufacturers, when N digits are multiplexed, each digit requires .85N times the rated continuous current to obtain the same apparent brightness. The desired L.E.D. brightness requires a constant current of five milliamperes per segment. When multiplexing is used for eight digits, the required current (I_f) per segment becomes:

$I_f = (.85)\ (N)\ (.005) = (.85)\ (8)\ (.005)$

$= .034$ amperes (Eq. 3-1)

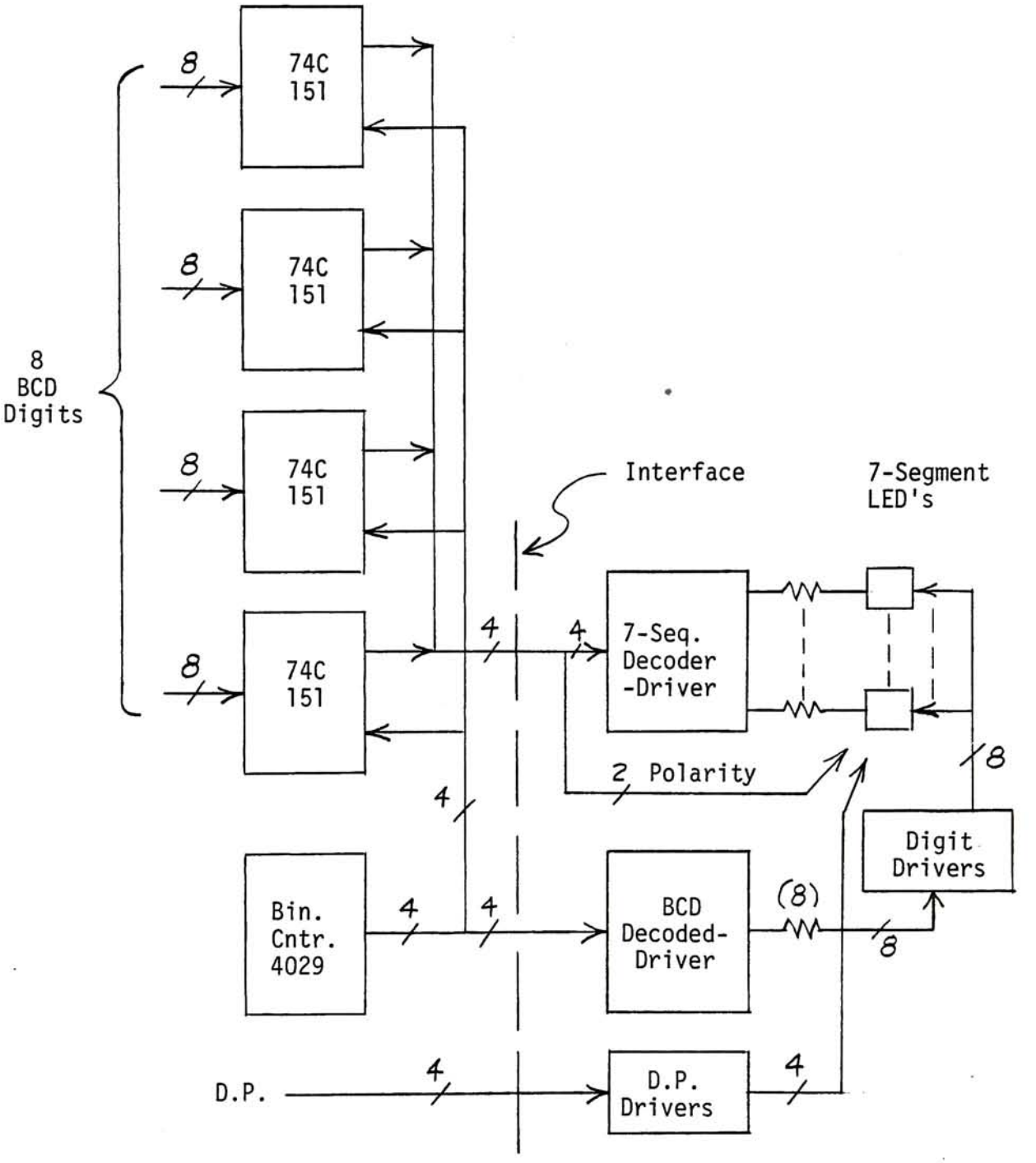


Figure 3.10 (b) Multiplexed Interface to the 7-Segment Data Display.

The total digit power requirements is then:

$7\ I_f\ V_{cc} = (7)\ (.034)\ (5) = 1.19$ watts

or 149 milliwatts per digit, where V_{cc} = positive logic supply voltage. The Texas Instruments SN7446A is a BCD-to-seven-segment decoder/driver with each output capable of sinking 40 milliamperes. The Texas Instruments SN7445 BCD-to-decimal decoder/driver is required to drive the digits via digit driver transistors. Both I.C.'s require a total power of 535 milliwatts. Since the National MM74C151 eight channel digital multiplexer and the RCA CD4029A presettable up/down counter requires negligible power, the total power (P_t) per digit is then:

$P_t = I_f\ V_{cc} + .535/8 = .149 + .067$

$= .216$ watts per digit (Eq. 3-2)

The multiplex control costs approximately $22.00, or $2.75 per digit. Each digit costs $2.25, therefore the total cost is $5.00 per digit. This cost and power dissipation is equal to the previous design approach, but requires less P.C. board real estate and much less interface wiring. This design approach will then be used.

The detailed design of this function can be accomplished at this time because its operation is not system-dependent. Figure 3.11 shows this sub-system design. Note that the transistors and resistors are in I.C. form, and that no discrete components are mounted directly on the P.C. board. This requirement makes it very convenient to replace defective components because all components are mounted in I.C. sockets.

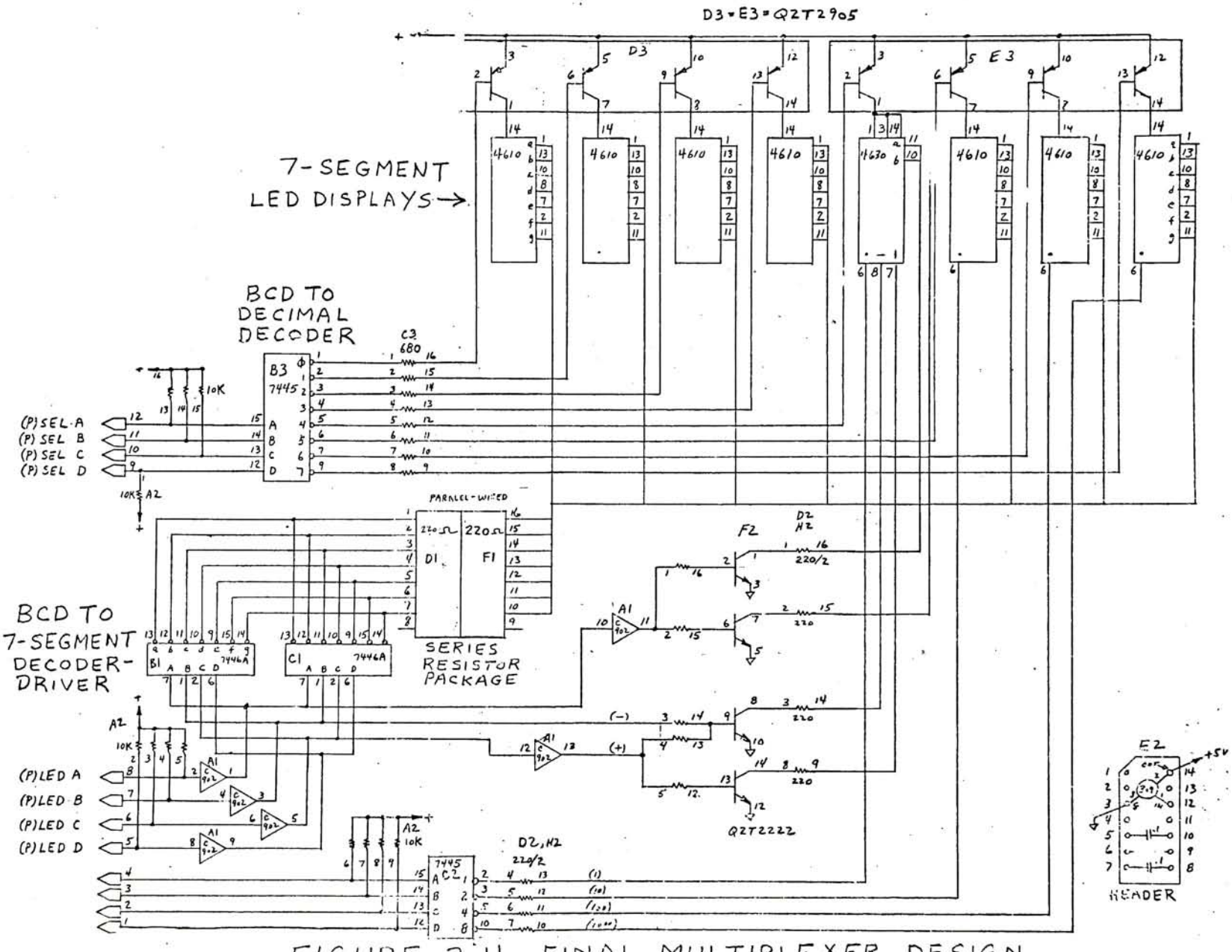


FIGURE 3.11 FINAL MULTIPLEXER DESIGN

3.2.3 Selection of the Data Channel Monitor Sub-System

The data channel monitor consists of the channel number selection and the data display. Figure 3.9 shows the location of the data channel monitor. The design of the channel number counter must be carefully selected because this counter is an integral part of the data acquisition sub-system.

A number of system requirements must be considered before this sub-system design can start. First, the data channel number must be displayed in decimal form. This dictates that the data channel counter is a two digit BCD type or a five digit binary type which requires a binary/BCD converter. A second requirement is that all analog multiplexers require a binary-coded channel select. The analog multiplexer is required in the A/D sub-system. A third system requirement is to sample all channels every 100 milliseconds, at a rate of 1.0 millisecond per channel. This requirement dictates that a counter must count from Ø to 99 (milliseconds).

Figures 3.12 and 3.13 show a solution with binary and BCD counters respectively.

Both solutions appear to require the same number of functions and the same I.C. count. The I.C. count would be equal if the BINARY/BCD converter (Fig. 3.12) required one I.C. such as the 74185A, or its equivalent in CMOS. The problem here is that the CMOS equivalent of the 74185A

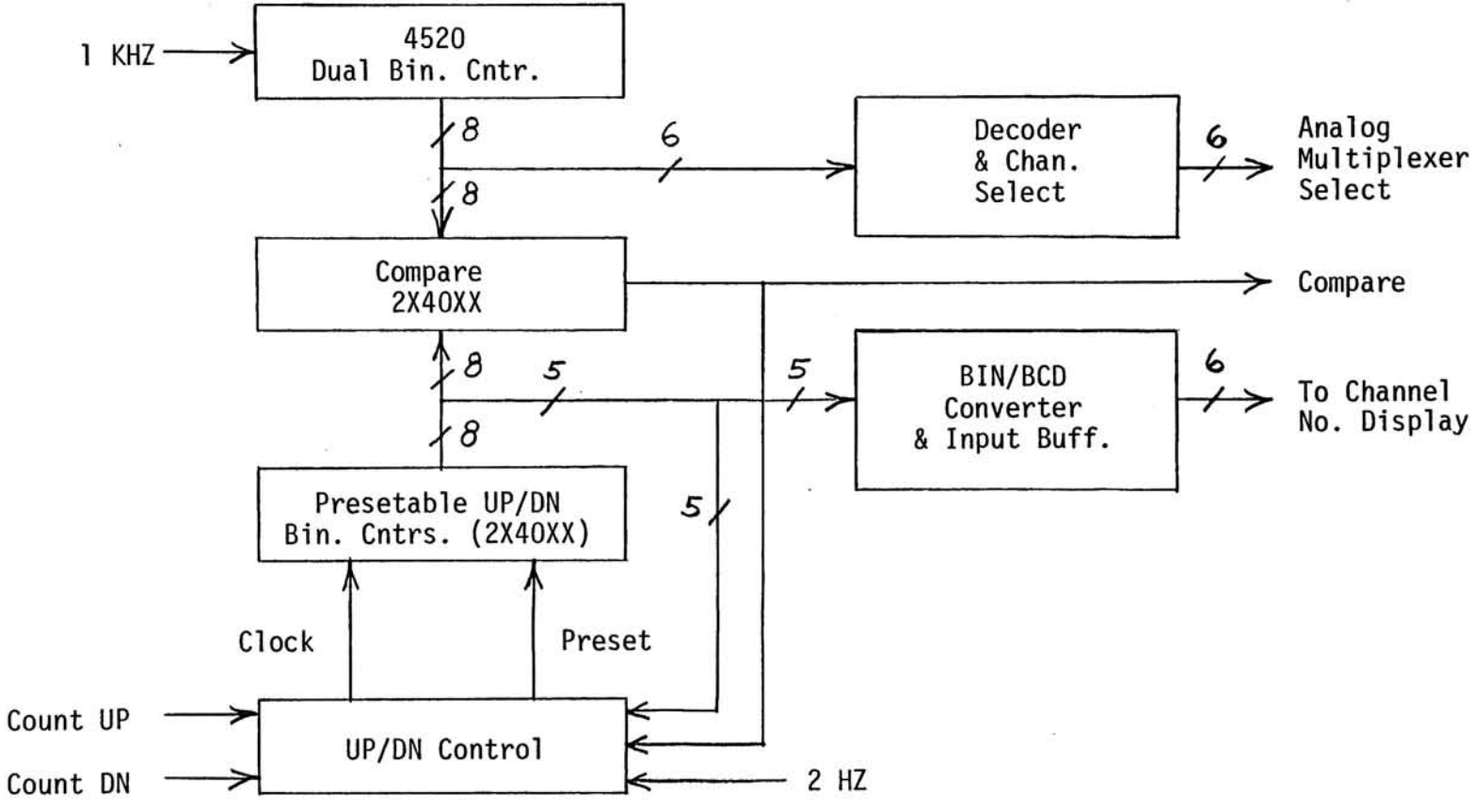


Figure 3.12 Data Channel Monitor Control with Binary Counters

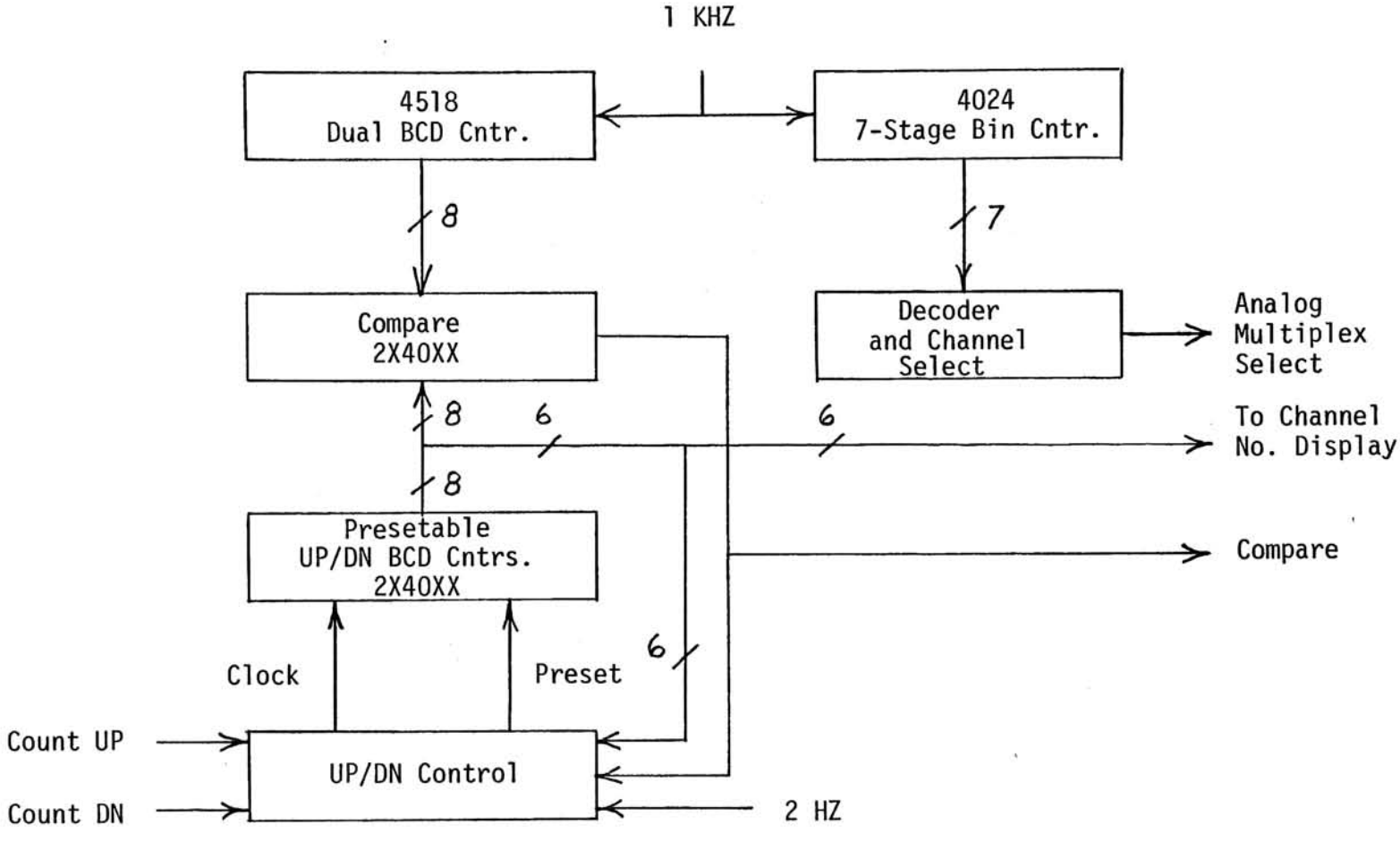


Figure 3.13 Data Channel Monitor Control with BCD Counters

is not available yet. The 74185A can be used by paying the penalty of adding five non-inverting buffers such as the National MM74C902 hex buffer I.C., and accepting the high power dissipation of the 74185A (300 mw). The system shown in Figure 3.13 is therefore the more favorable of the two solutions and will be selected for the data channel monitor sub-system.

3.2.4 Selection of the Data Tolerance Memory Sub-System

The data tolerance requirement is defined in paragraph 3.1.9, page 6 . The data tolerance can be selected on the Control Panel shown in Figure 3.9. The displayed data tolerance is the tolerance for the displayed Channel Number. The data tolerance for any data channel can be changed by first selecting that data channel on the Control Panel display, then incrementing or decrementing the Data Tolerance display by activating the UP or DN (down) switches respectively, until the desired tolerance is displayed. The selected data tolerance number is stored in memory along with the data tolerance numbers for each of the other data channels. If the data tolerance memory is accessed for all 20 data channel tolerances once every 100 milliseconds, then the tolerance of the monitored data channel must be stored in a register which can be multiplexed to the tolerance display on the control panel.

The decision to use binary or BCD for the counter (and storage) must again be considered. The system requirement specifies that a range of Ø thru 15 percent be used with Ø representing a display of 99 percent, indicating an OFF condition for the selected channel tolerance. Zero thru 15 is easily obtained by a standard four-bit binary counter. Two 16 word x 4 bit/word MM74C14 RAM I.C.'s (National) can be used to store the 20 data channel tolerances. Figure 3.14 illustrates the functional requirements for the data tolerance memory. The sub-system is initialized with a RESET when power is turned on. During RESET the presettable UP/DN counter is at count zero, causing the memory to store zero in each data channel memory location. Upon termination of RESET the counter will increment UP or DOWN (DN) when the channel compare is true (see Fig. 3.13) and the UP or DN touchbuttons are activated respectively. Each time a data channel is selected the corresponding tolerance is read from memory and preset into the counter. It is then incremented, decremented, or neither and re-written into memory.

The BINARY/BCD converter performs the functions shown. Note that three functions are performed by this converter. This sub-system will be designed in detail in para. 5.1.2.

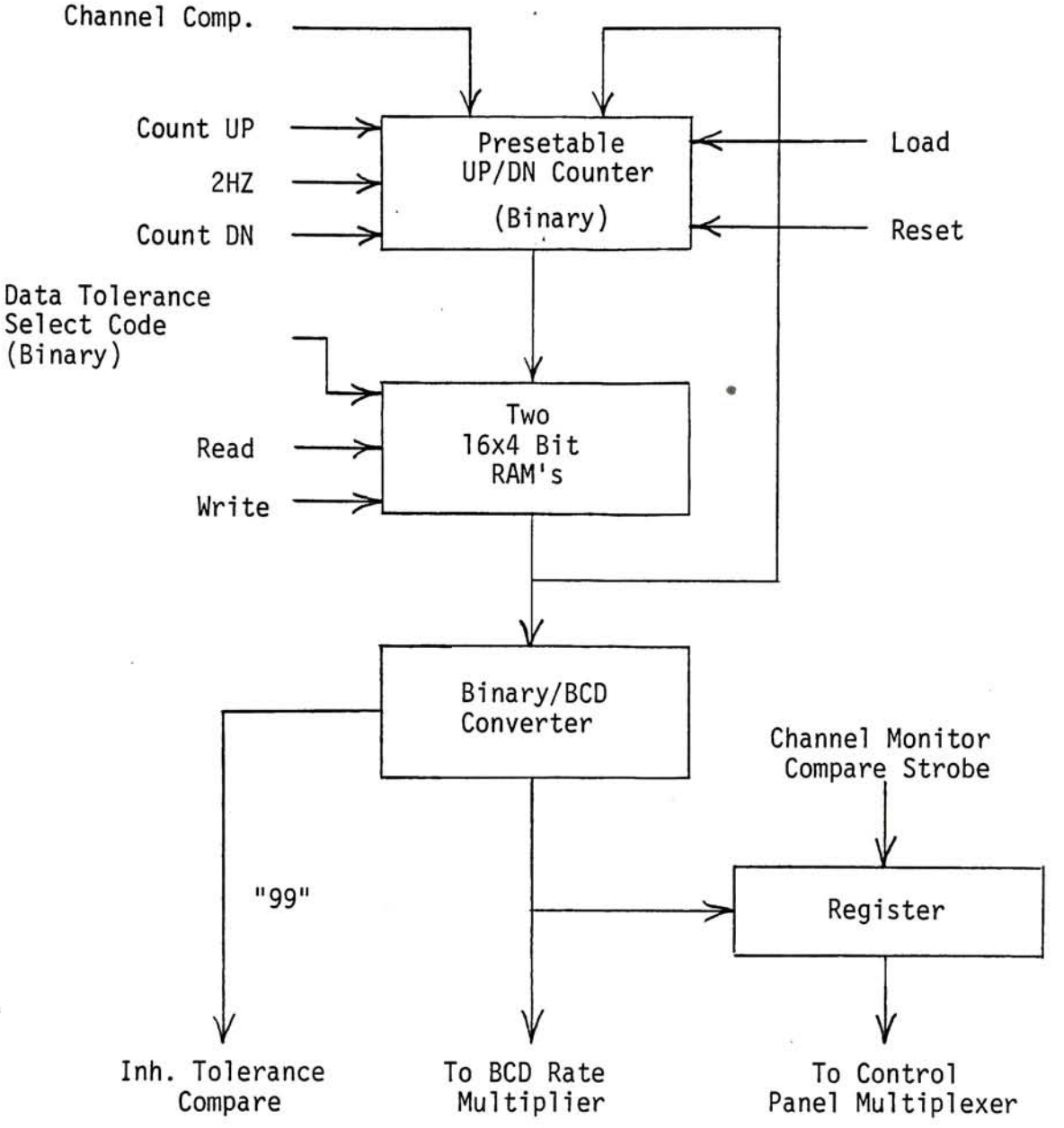


Figure 3.14 Data Tolerance Memory

3.2.5 Selection of the Data Compression Rate and Sample Rate Sub-Systems

Four Data Compression rates and four Fixed Data Sample rates are selectable on the Control Panel shown in Figure 3.9. Only one rate can be selected in each group. This can be accomplished with a digital-interlock register design for each group. Four momentary-action switches are required for each data rate group, as shown in Figure 3.9.

When a specific Data Compression rate is selected, the maximum printout is determined. As an example, if two samples per second is selected, then each data channel is sampled at that rate and printed when one or more channels goes out of tolerance.

When a specific Fixed Data Sample rate is selected, then all data will be printed at the selected sample rate.

A "LOCK" switch is provided on the control panel. Activation of this switch inhibits all sample rate switches from accidental activation. A "Data Request" switch is located next to the LOCK switch, and causes one line of data (from all channels) and time to get printed each time it is activated.

Figure 3.15 shows the functional block diagram of the Sample Rate sub-system. There are a number of ways to design an interlock register (Reg. #1 and 2). Figure 3.16 shows a solution requiring 6.25 I.C. packages. The four R-C networks are considered as one I.C. because they can be mounted on a 16 pin component header and inserted into an I.C. socket. Figure 3.17 shows an interesting configuration with a resistor tied from the F/F output (Q) to the data input (D). The total resistance of R1 and R2 is important for proper operation, and depends upon the

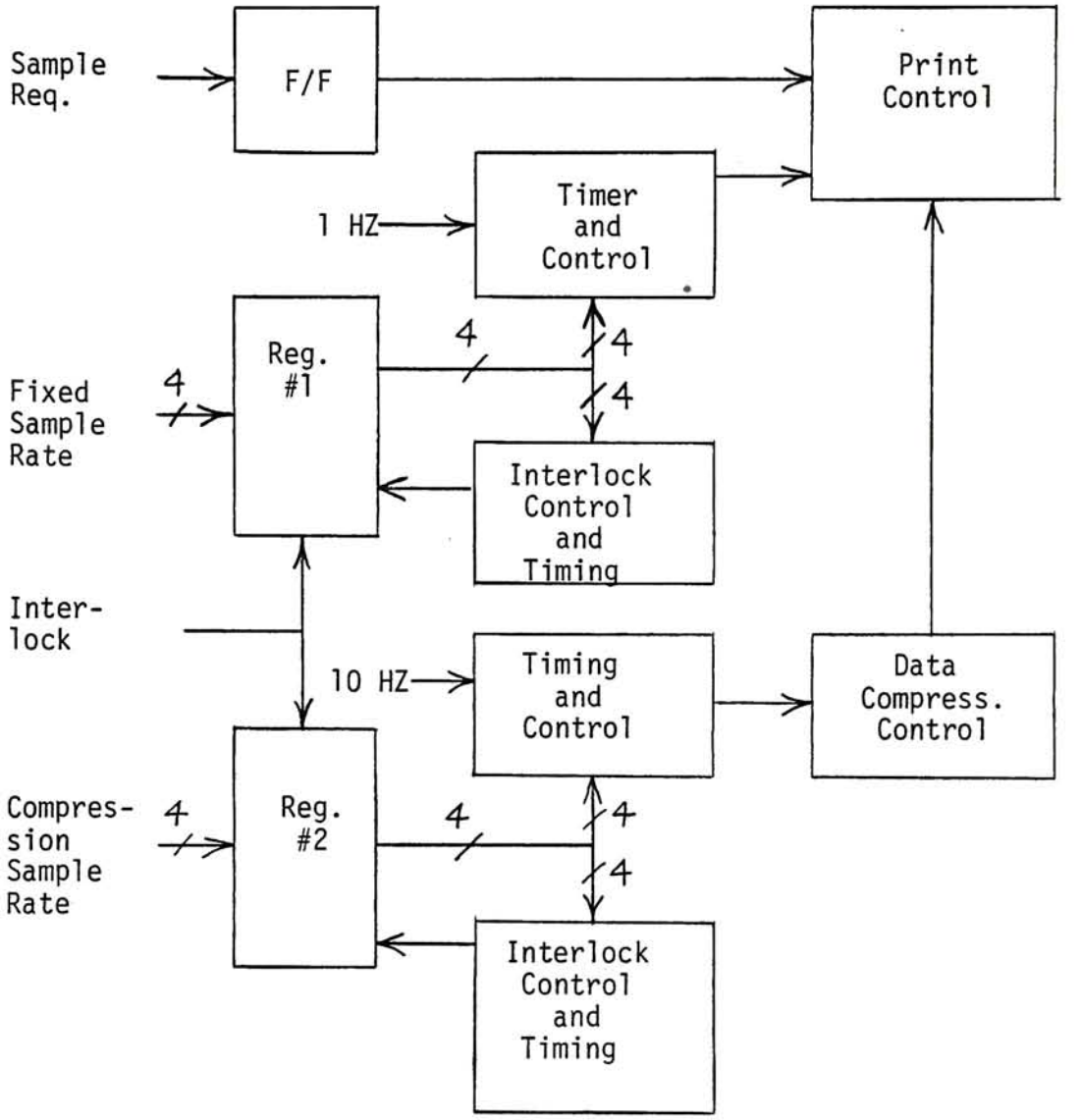


Figure 3.15 Sample Rate Sub-System

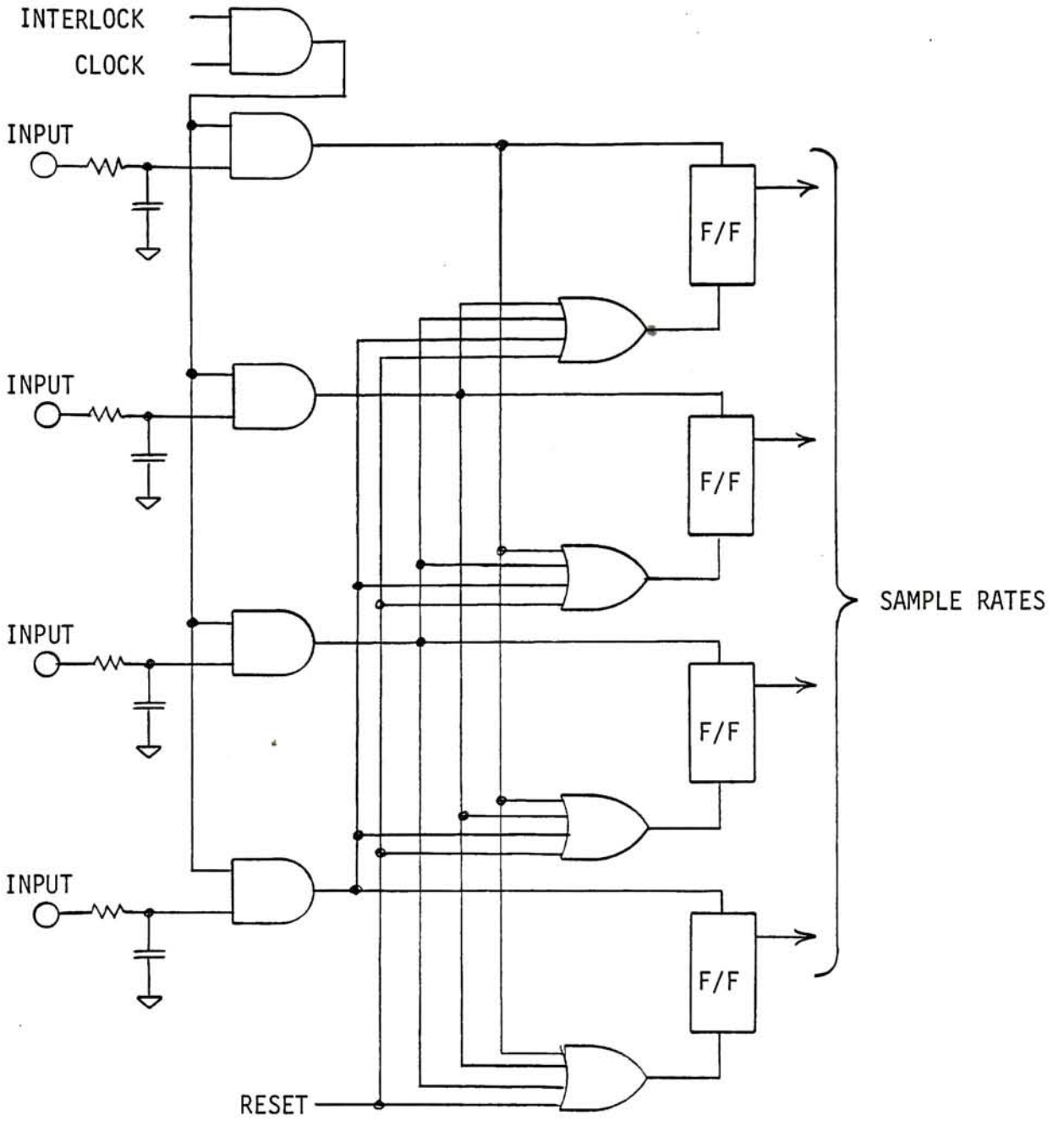


FIGURE 3.16 SAMPLE RATE REGISTER NO. 1

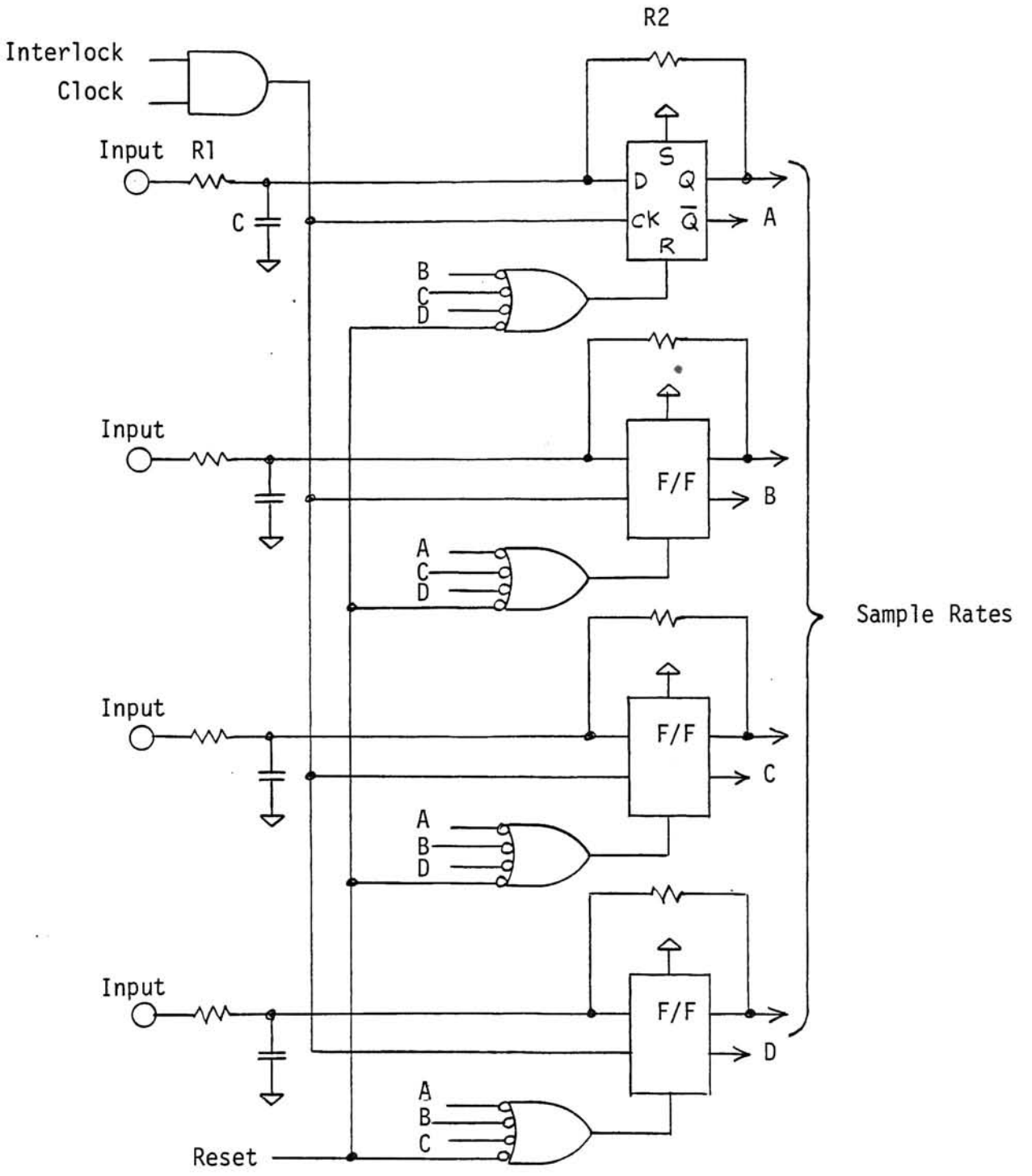


Figure 3.17 Sample Rate Register No. 2

input voltage, resistance (human finger), and the type of F/F used. A safe value which can be used with CMOS logic is a minimum of one megohm. For an input voltage of 20 VDC and a maximum source resistance (human finger) of 10 megohms, an input current of 1.64 microamperes flows thru R1.

The function of the input capacitor (C) at R1 of Fig. 3.17 is to protect the CMOS input from static discharge that may be transferred from the operator's finger. I have empirically selected a .01 microfarad capacitor with a current-limiting value of 47,000 ohms for R1 and 4.7 megohms for R2. With this combination the CMOS input will clamp at +5V (approximately) and the Q output of the F/F must sink 1.06 microamperes.

The solution shown in Figure 3.17 decreases the total I.C. package count to 5.75. A third solution which requires only one 74C175 quad F/F instead of two 34013 dual F/F's is illustrated in Figure 3.18. This used a 74C42 BCD-to-decimal decoder and a four-input NOR gate to enable a reset of the 74C175 if the number is true (high) Q outputs is zero or greater than one. This is accomplished by tying the 1, 2, 4 and 8 decoded outputs of the 74C42 to the four-input NOR gate. The total I.C. package count of this solution is 4.5, making it the best choice. This design can be used for REG. #1, REG. #2, and the associated "interlock control and timing" function (Figure 3.15).

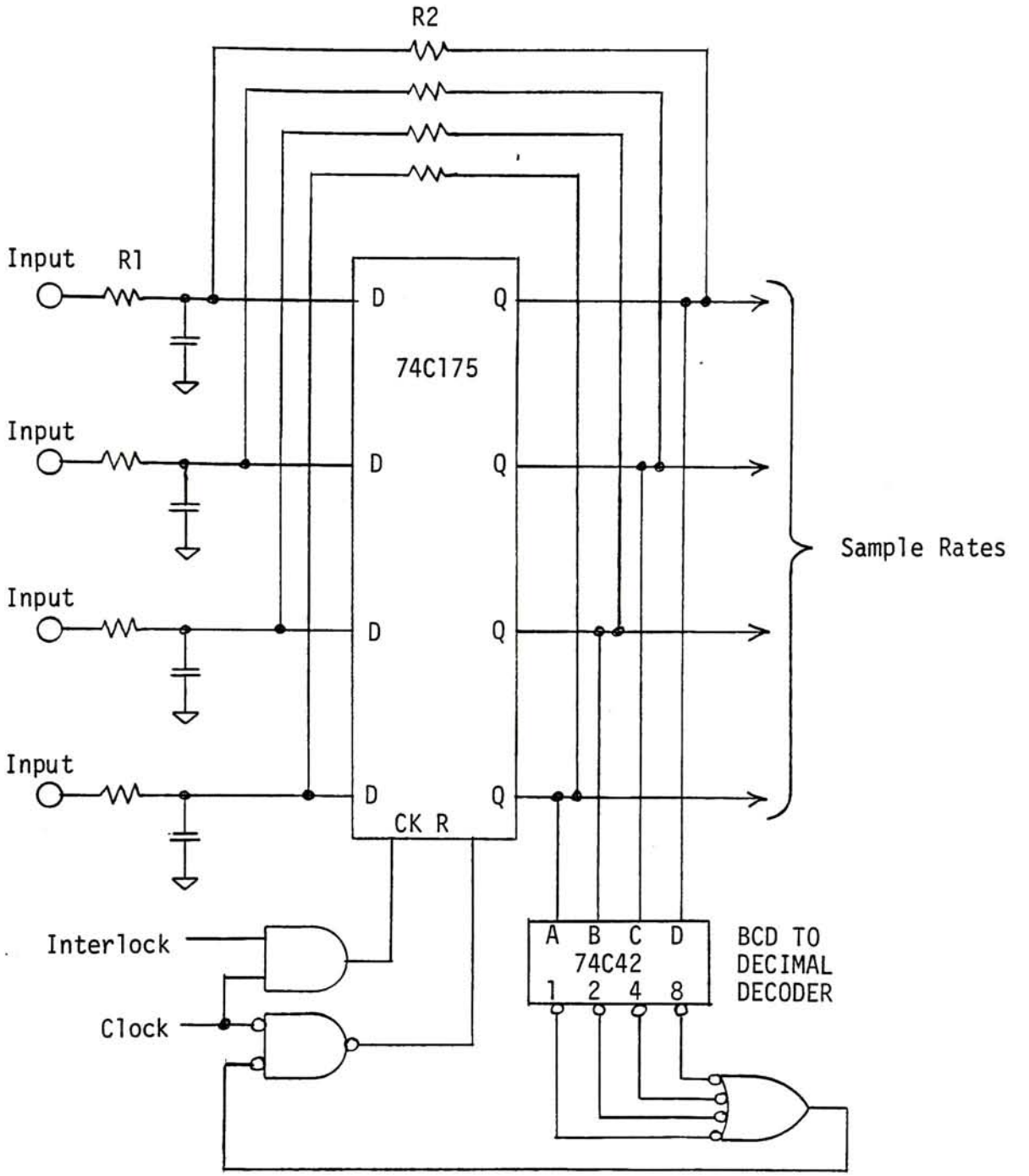


Figure 3.18 Sample Rate Register No. 3

3.2.6 Selection of the A/D Conversion Sub-System

At this point the requirements of the A/D conversion sub-system have been defined as follows:

- The analog multiplexer shall multiplex 20 data channels and three voltage references to the A/D converter.
- A polarity output for the control panel data display and the Versatec line printer (in ASCII code) shall be provided.
- An output pulse train (count) which is equal to the converted data value. This is required for the BCD rate multiplexer function.
- The A/D converter output shall be in binary code as required by the data compression sub-system.
- The A/D converter output shall be in 3-1/2 digit BCD code as required for the control panel data display.
- The A/D converter output shall be in ASCII code as required by the Versatec line printer.
- The total A/D conversion accuracy shall be $\pm$ .05 percent, $\pm$ 1 L.S.B.

A dual slope A/D converter can be selected from numerous companies as a single-packaged module or in two or more packages. The problem with a single-packaged module is conversion speed. The fastest single-package dual slope A/D converter is made by Teledyne Philbrick and is their model 4111[4]. This model is a 3-1/2 digit, integrating A/D converter which has a number of disadvantages such as high cost ($94.00 in small quantity), three highly regulated power supply voltages ($\pm$ 15V $\pm$ 1%, + 5V $\pm$ 2%), high total power (1.65 watts), no output pulse train (required

for the BCD rate multiplier), and a conversion time of 2.5 milliseconds. The conversion time and the lack of an output pulse train makes this, and all other units, impossible to use.

Two-unit integrating A/D converters are another possibility. A common two-unit combination consists of an analog unit and a mating digital unit. A number of I.C. manufacturers are introducing low-cost two-I.C. integrating A/D converters. Motorola has a MC1405L/MC14435[5] I.C. pair which operates with a single supply voltage of 5-15 volts and requires a total nominal power of 44 milliwatts at 5 volts.

At this point it is important to explain the principle of operation of an integrating A/C converter. The dual ramp method of A/D conversion is a proven system which is capable of very high accuracy. Figure 3.19 illustrates one A/D conversion cycle of a dual ramp A/D converter. The conversion is an integrating process which offers high noise rejection and immunity to change in the clock rate and integrating capacitor value. The charge of the integrating capacitor is proportional to the input voltage to the A/D converter. An offset current source is added to the charge current. The addition of this offset current guarantees that the ramp does not have a zero slope when the input voltage is zero, and allows reliable conversion at low input voltages by providing a good ramp signal-to-noise ratio.

The discharge current arbitrarily is set to one-half of the maximum charge current rate (due to the input voltage only). This means that if the integrating capacitor is allowed to charge for 1000 clock counts at the maximum current of $(I + I_o)$, where I is the current due to the input voltage to the A/D converter and $I_o = .05I =$

(4) Teledyne Philbrick Product Guide 76, pp. 22 & 23.
(5) Motorola, Inc. 1975, Application Note AN-748.

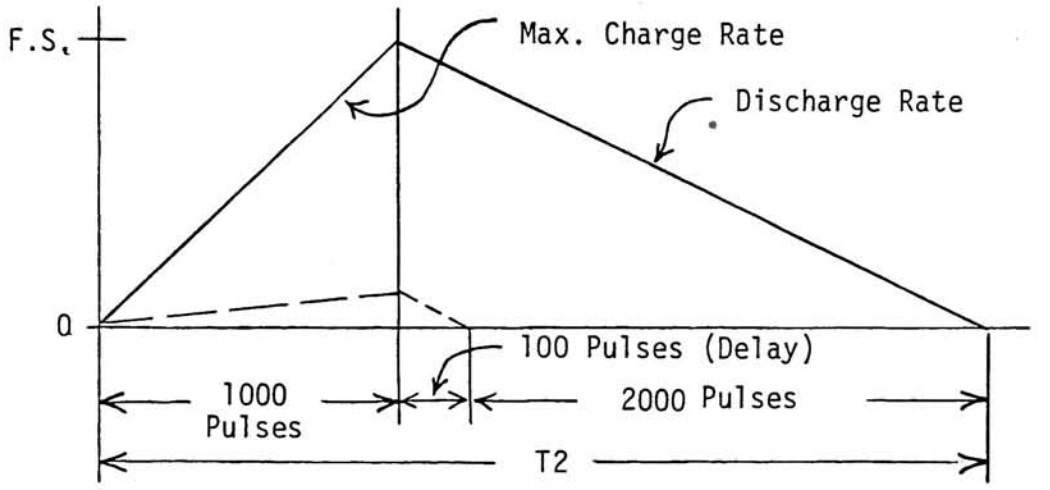


Figure 3.19 One A/D Conversion Cycle

offset current, then the total capacitor charge is proportional to 1000 $(I + I_o)$. If the discharge current is half of the maximum charge current (I), then the time required for the capacitor to discharge is proportional to T_D (I/2), where T_D is the number of counts required for the capacitor to discharge. The capacitor charge must be equal to the discharge, therefore: 1000 $(I + I_o)$ = T_D (I/2) or: $T_D = 2$ [1000 $(I + .05I)/I$] = 2100 clock counts.

The ramp offset current accounts for 100 of the 2100 clock counts. This "offset count" is compensated by the digital logic so that it does not appear in the counter which holds the A/D conversion value at the end of the conversion cycle. The MC14435 logic sub-system has a maximum clock frequency limit of 1.0 megahertz. Assuming that one-half of the total channel select time of 1.0 millisecond may be used for A/D conversion, and that a built-in count delay of 100 pulses is used to compensate for the offset current (see Figure 3.19), then the required frequency (f) for a 3-1/2 digit conversion is: $f = T1^{-1}$ where T1 is the period of count pulses in Figure 3.19. Figure 3.19 shows that the maximum number of T1 counts for time T2 is: T2 = (1000 + 100 + 2000) T1 = 3100 T1. Also, T2 = 500 x 10^{-6} sec. = max. conv. time. $\therefore$T2 = 3100 T1 = 500 x 10^{-6} sec. then T1 = 500 x $10^{-6}/3100$ sec. = .1613 x 10^{-6} sec. and $f = T1^{-1} = (.1613 \times 10^{-6})^{-1}$ = 6.2 x 10^6 Hz.

This frequency is too high for the MC14435. This does not eliminate the possibility of using the MC1505L analog-to-digital converter sub-system, which is capable of converting to 13 bits with a count frequency limit which is dependent on the speed of the logic used for the digital sub-system. The digital sub-system can include a BCD counter for the primary A/D conversion function, a binary counter to obtain the binary A/D value, a BCD-to-ASCII converter for the printer requirement, and the required pulse train for the BCD rate multiplier requirement.

Up to this point a dual slope A/D converter was referred to as the solution to an integrating type A/D converter. Another method which warrants attention is a voltage-to-frequency (V/F) converter. A V/F converter outputs a pulse train whose repetition rate is linearly proportional to an analog input voltage. Figure 3.20 shows a simple block diagram of an integrating A/D converter sub-system with the required BCD, binary, and ASCII conversions.

This sub-system requires a divide-by-eight counter after the gated pulse train from the V/F converter because the pulse train does not start synchronous to the start converse pulse. The frequency at "A" (Figure 3.20) is then synchronous to the start convert pulse with an error

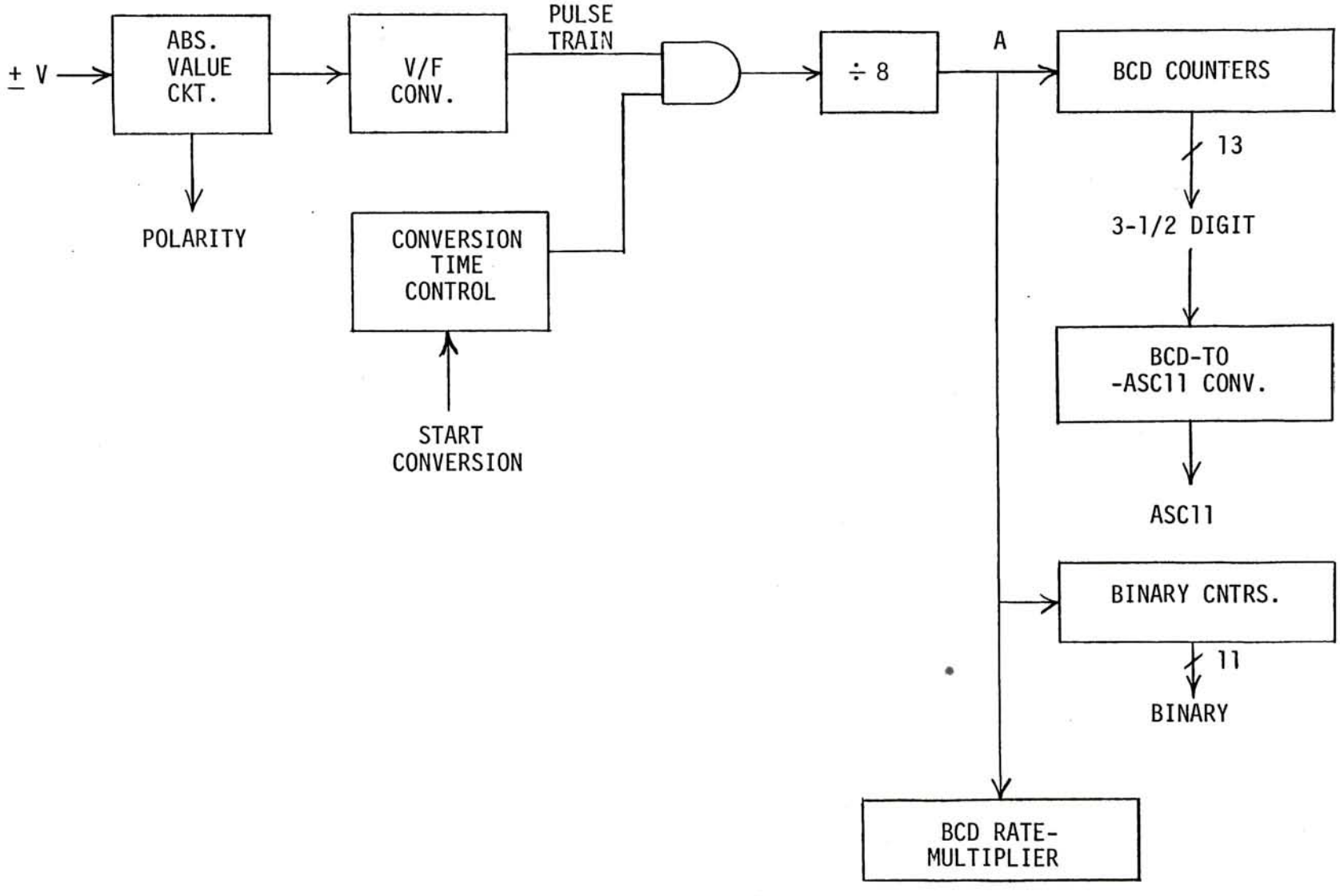


Figure 3.20 V/F Converter Sub-System

of $\pm$ 1/8 count. Another requirement is that the "conversion time control" function requires a crystal oscillator time-base to obtain an accurate gate time for the V/F output pulse train.

With the addition of a divide-by-eight counter, the V/F converter must have a maximum frequency of $8 \times 6.2 \times 10^6$ Hertz, or 49.6×10^6 Hertz. The highest frequency V/F converter is a 5 megahertz (F.S.) unit made by Teledyne Philbrick. This unit (4707-02) sells for $186.00 in 10-24 quantity. This unit can be used without the divide-by-eight counter only if an additional tolerance of $\pm$ 1 count could be tolerated and a conversion time of $3100/5 \times 10^6 = 620 \times 10^{-6}$ seconds can be tolerated. Even if the 620 microseconds could be tolerated, the $\pm$ 1 count increases the total tolerance by ($\pm$ 1) (100)/1999 = .05%, which is unacceptable.

The final selection of an integrating A/D converter will be the Motorola MC1405L dual ramp A/D converter with discrete I.C.'s used for the digital portion of the sub-system. Figure 3.21 shows the complete dual slope A/D converter sub-system. A wide selection of analog multiplexers are available and will be selected in the digital design. The remaining portion of the sub-system is also straightforward and will be designed later.

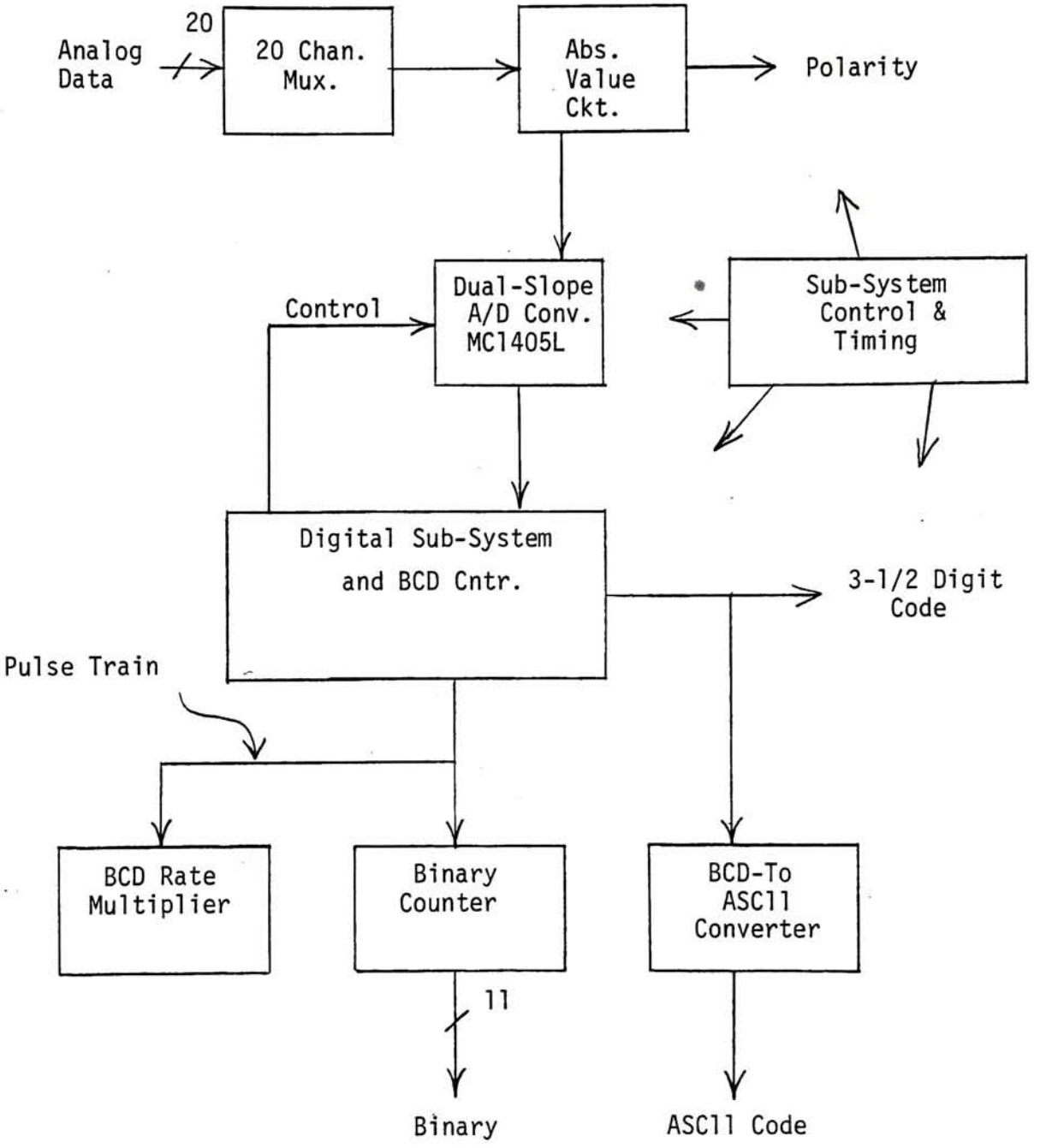


Figure 3.21 Dual-Slope A/D Converter Sub-System

3.2.7 Selection of the Data Channel Interface Sub-System

This sub-system receives all analog and digital data and performs the required function(s) with this data to transmit it to the system control electronics in the required form. The analog signals must be transmitted in a voltage range of -2,000 volts to +2.000 volts and the digital data must be transmitted in BCD code and in the ranges of -1999×10^{-N} to $+1999 \times 10^{-N}$ where N = 0, 1, 2 or 3. This sub-system consists of 10 data modules. Each data module can contain two analog channels, two digital channels, or one analog and one digital channel.

The interface between the system control electronics and the analog/digital data modules must include the following functions:

- Multiplexed analog interface.
- Multiplexed digital interface.
- System clock interface.
- Any additional interface requirements as found necessary during the interface design.

The ideal system will enable any analog or digital plug-in module to be used in any one of the 10 available locations. This can be accomplished with a bus-oriented backplane. The additional requirement that each plug-in module have two data channels further defines the backplane requirements.

The basic block diagram of the interface is shown in Figure 3.22. Each of the four interfaces can be fully or partially multiplexed, decreasing the total number of interface lines required. Analog data can be multiplexed on the analog modules as shown in Figure 3.23 (a). Each analog channel requires an individual analog "switch" for this configuration. The penalty for multiplexing is the requirement for a multiplex select code, which costs in added logic and interface wiring. The select code can also be used to enable the selected channel to indicate if it is analog or digital. The digital channel must also indicate if it has valid digital data. This can be accomplished by adding a multiplexed "digital valid" signal on the bus. The decision must now be made to send a decoded or encoded channel select to the modules. Twenty channels require a five-bit select code which can be decoded on each of the ten modules or decoded at the transmit end and individually wired (20 wires) to each module. The first approach not only requires a decoder on each module, but also requires each module to have the capability of channel selection. This method is undesirable because the same channel can be accidently selected on two or more modules. The second approach requires fifteen more wires than the first, but is more desirable because of lower cost and the guarantee that only one channel at a time will be selected.

The digital data channels will be capable of transmitting a signed 3-1/2 digit BCD value. This requires 14 lines for transmission. Figure 3.24 (a) shows the interface required for

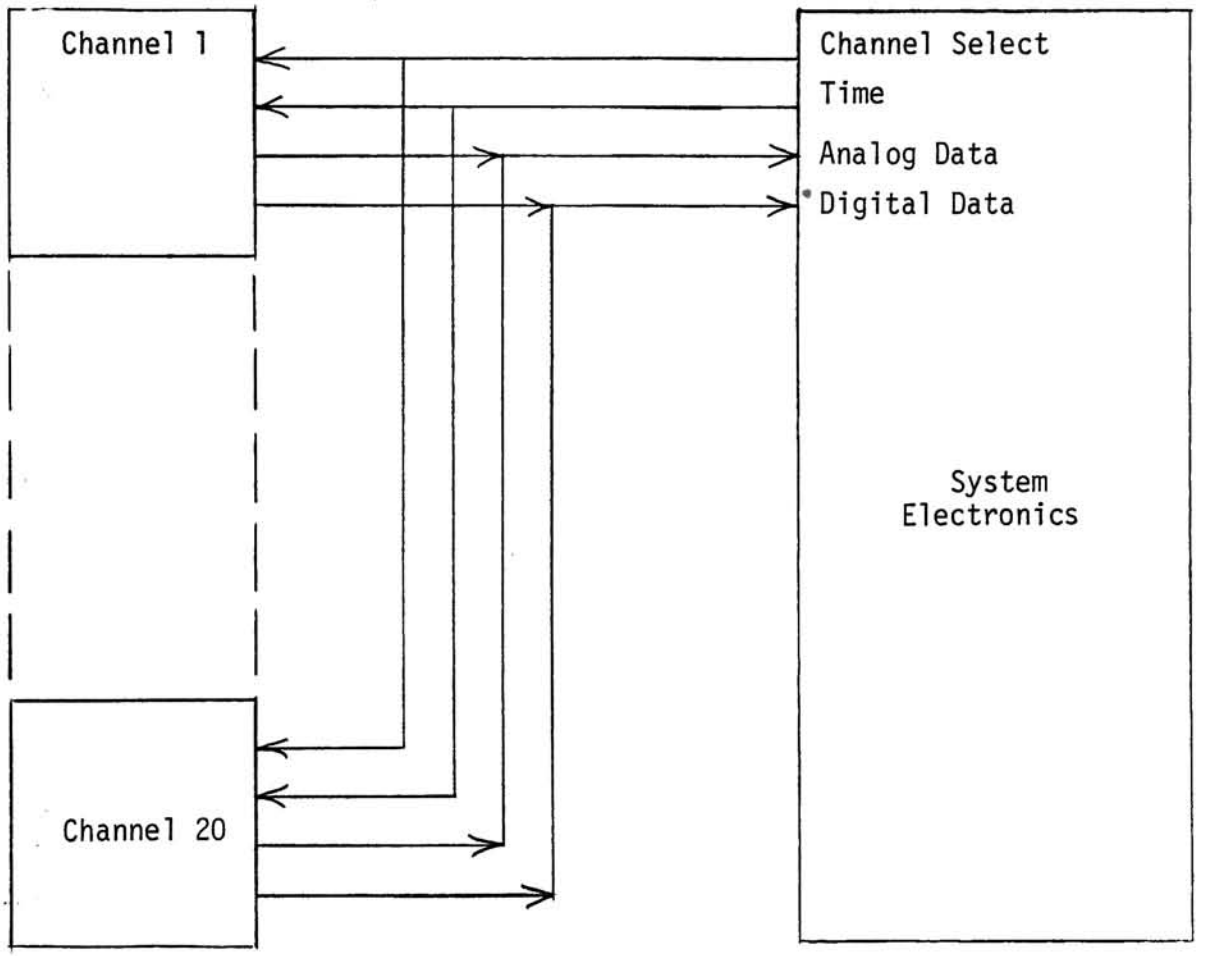


Figure 3.22 Basic Module Interface

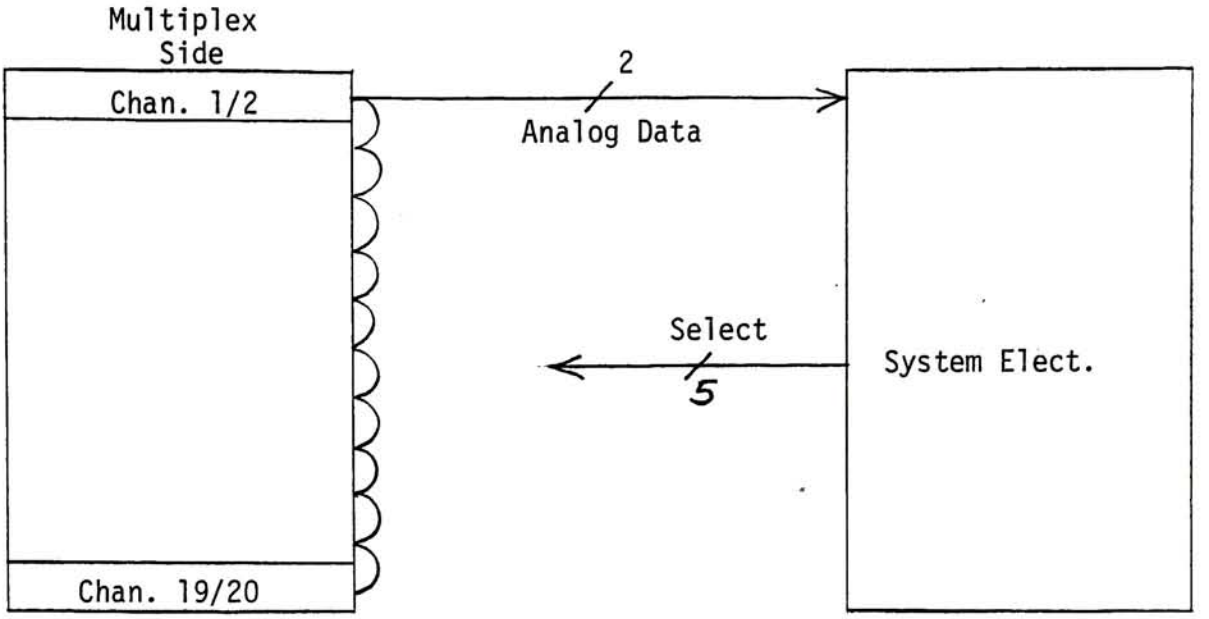


Figure 3.23(a) Module-Side Analog Multiplexing

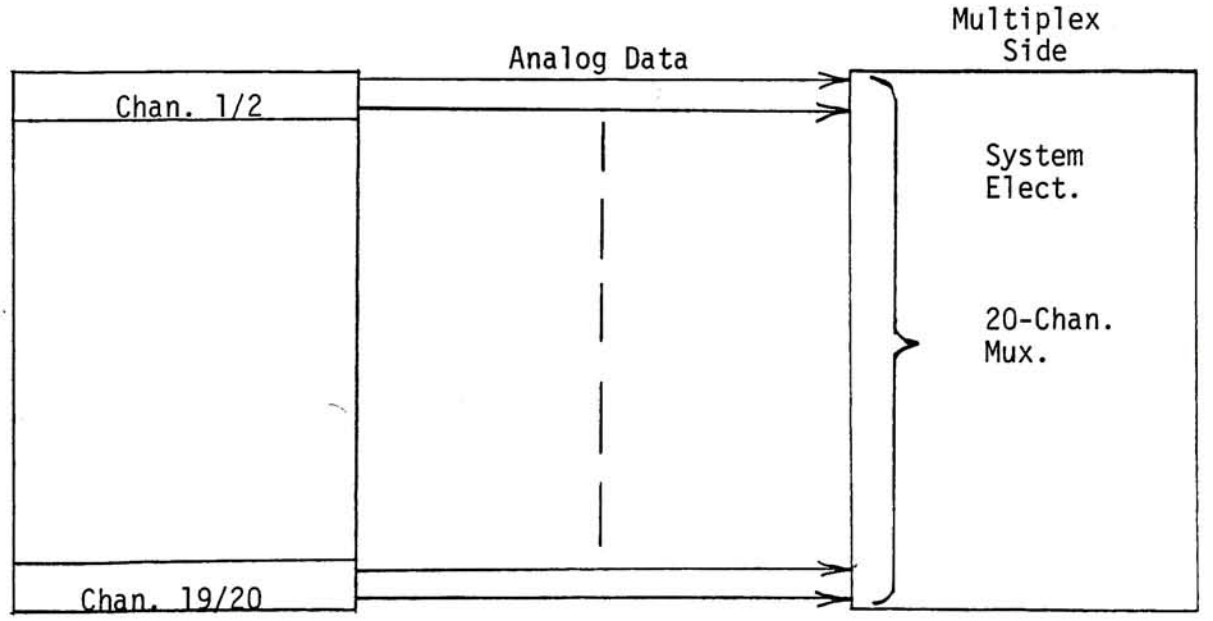


Figure 3.23(b) System-Side Analog Multiplexing

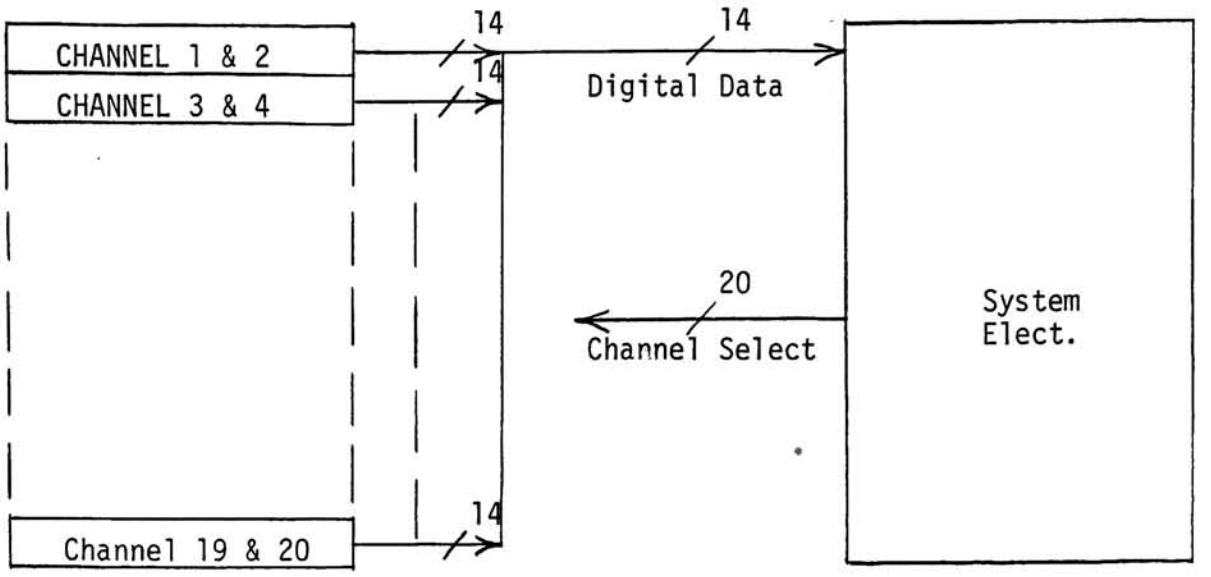


Figure 3.24(a) Multiplexed Parallel Digital Data

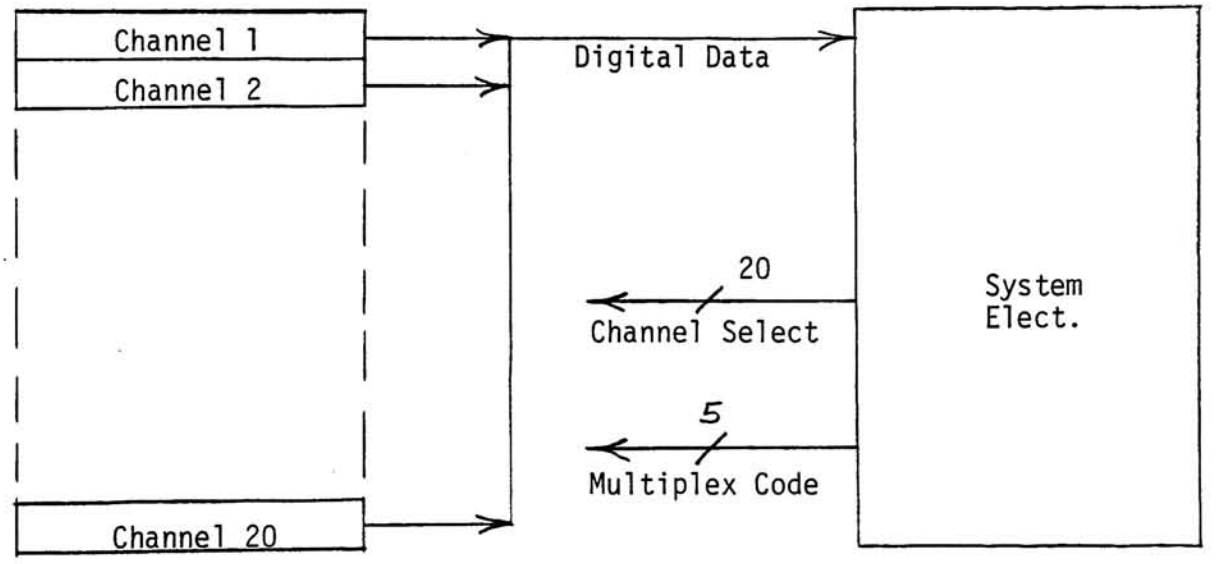


Figure 3.24(b) Multiplexed Serial Digital Data

multiplexing 14 lines of digital data from each of 20 channels. This method requires partial multiplexing (two channels) on each board plus 126 backplane wires and 14 interface wires. If the digital data is transmitted in serial form as shown in Figure 3.24 (b) then the total wire count is reduced to 10. This advantage must be paid for by the addition of a four-bit code which is required to multiplex the 14-bit digital data.

Figure 3.25 shows a method for multiplexing digital data from a module which contains two digital data channels. Note that the two channels are designated as channel-x and channel (X+1). These channels could be 1 and 2, 3 and 4, ... 19 and 20. The 16-bit digital data value is multiplexed from both 4512 multiplexers of either channel by sequentially multiplexing the data bits from the LSB to the MSB. The output of the 4512 (F) is tri-state. When the $\overline{OE}$ is high, the output is in the high impedance state. When $\overline{OE}$ is low, the output is equal to the selected data input bit.

One requirement for the digital data channels is to record the time of an event. This time must be derived from the system clock. Since each channel is scanned once every 100 milliseconds, a convenient clock frequency (count) would be 1KHz. This frequency enables timing of an event to the nearest millisecond, which is sufficient for most applications. Actually, since 16 bits of data may be transmitted, time could be decreased to .1 milliseconds per count (a 10 KHz frequency). This would require four BCD counters with an input frequency of 10 KHz.

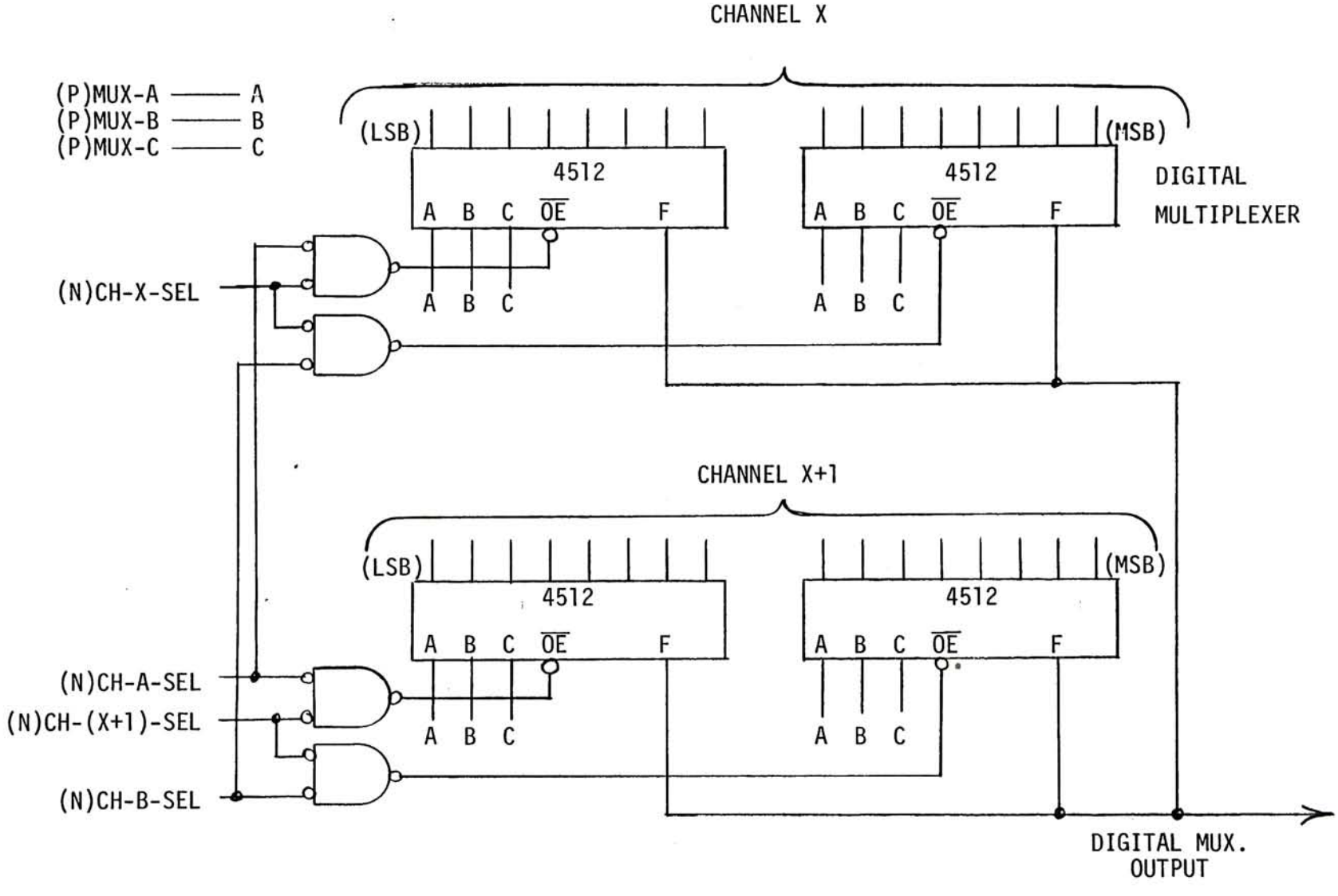


FIGURE 3.25 SERIALLY MULTIPLEXED DIGITAL DATA FIGURE

When an event does occur, the counter must be stopped and the DIGITAL VALID signal must go true, indicating to the system logic that digital data is available for printout. When transmission of the data is completed, a signal is required to reset the DIGITAL VALID flip flop and to preset (synchonize) the BCD counters to the system time. A 3-digit BCD counter is then required as a system reference. This counter output (12 wires) must be wired to each of the 10 modules. The same 1 KHZ clock which is used for the system counter must also be sent to each module. The signal which resets the DIGITAL VALID flip flop and presets the digital channel counter can also be used for other functions, such as a reset signal to a sample-and-hold circuit on an analog channel. Since it is desirable not to have logic on an analog card, each module will have two reset signals (one for each channel) named CHANNEL-SET-X and CHANNEL-SET-(X+1). Since this signal can be used as an analog reset, it must be transmitted after A/D conversion is complete.

The module connectors can be wired as shown in Figure 3.26. Note that the +10 VDC, +20 VDC, and -20 VDC is used to obtain -5 VDC, +12 VDC (or +15 VDC), and -12 VDC (or -15 VDC) respectively. On-board regulation eliminates system noise

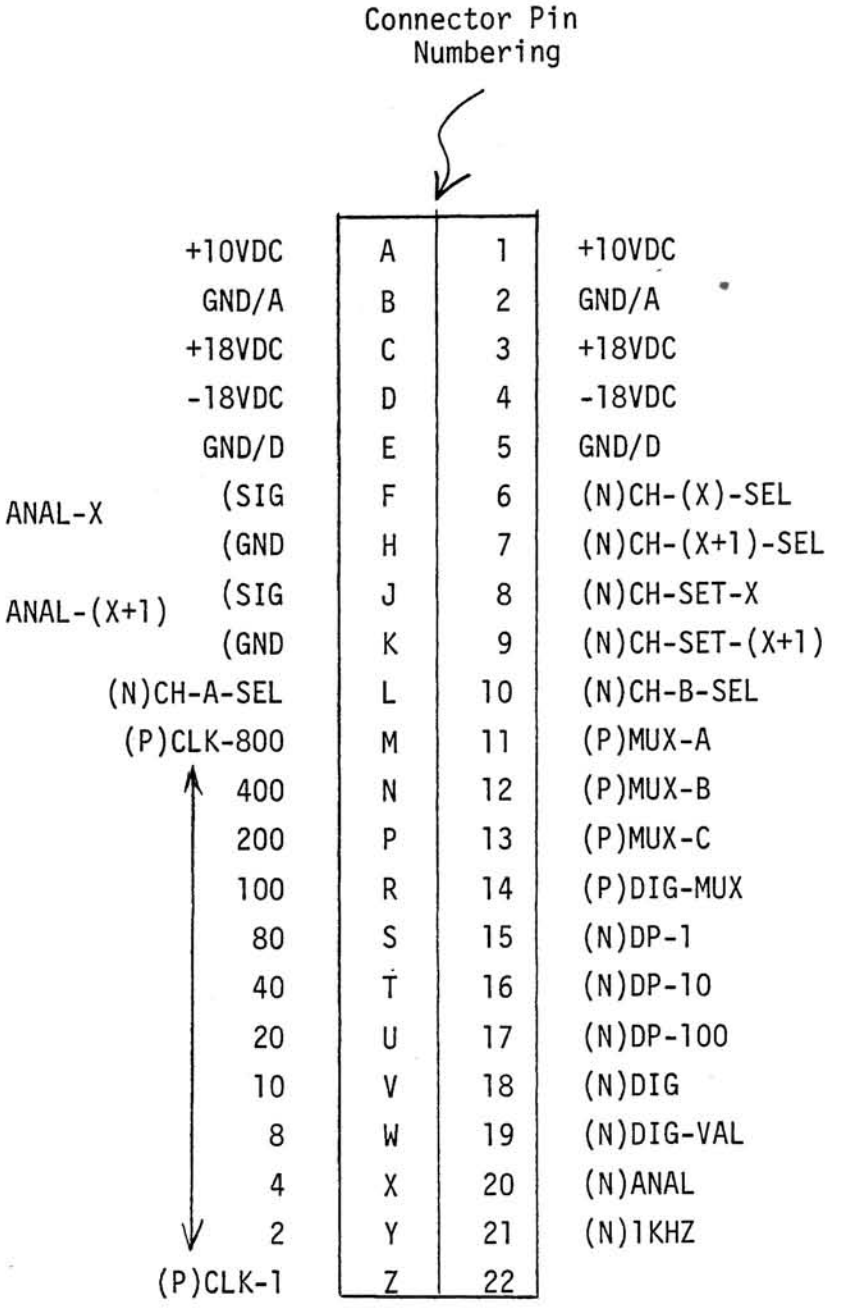


FIGURE 3.26 MODULE CONNECTOR SIGNALS

problems and also enables analog modules with power supply - sensitive circuitry to be interchangeable between systems without recalibration.

The only signals which are not bussed (common to all modules) are those signals which have an "*". This backplane is easy to wire and can be made of a printed circuit mother-board.

The polarity of a signal is indicated by an "(N)" before the signal name to indicate that it is "negative-true" or a "(P)" to indicate that it is "positive-true." In either case, the (N) or (P) indicates the "active-true" state.

The final system interface requirement is transmission of the decimal point location. The transmitted data will have a range of from Ø to 1999. Four decimal point positions are possible so only two lines are needed to indicate 1 of 4 decimal point positions. Because it is desirable not to have logic decoding on an analog board, another method must be found. Four lines can be used to indicate 1 of 4 decimal point locations. These lines can be named DP-1, DP-10, DP-100, and DP-1000. If the DP-1000 line is omitted, then it is implied to be true if the other three

lines are false (logic Ø). The total number of lines required for this function is then 3.

Figure 3.27 shows a dual-analog channel module with two AC/DC voltmeters, each with a selectable full scale input of 2V, 20V, 200V, or 2000V.

The voltage gain of the Analog Device's AD521J[6] differential amplifier is:

$$GAIN = R_f/R_{IN} \qquad \text{(Eq. 3-3)}$$

The 15K ohm potentiometer is required to obtain an approximate value of 100K ohms for R_f. The selected R_{IN} value can produce a gain of .1, 1.0, 10, and 100 by selecting 1M ohm, 100K ohms, 10K ohms, and 1K ohms respectively. The input resistance divider of 100 also provides input protection for the amplifier. This divider causes the overall amplifier gain to be .001, .01, .1, and 1 respectively. As an example, selection of R_{IN} = 1M ohm is required when a full scale input of 2000V is desired. The gain for this selection is .001, producing a full scale amplifier output of 2V. Switch SW1 (SW2) is located in two positions - gain selection and decimal point selection. For the given example, output pins 15-17 are all high.

(6) Analog Devices, Inc., Product Guide 1975, pp. 196, 197.

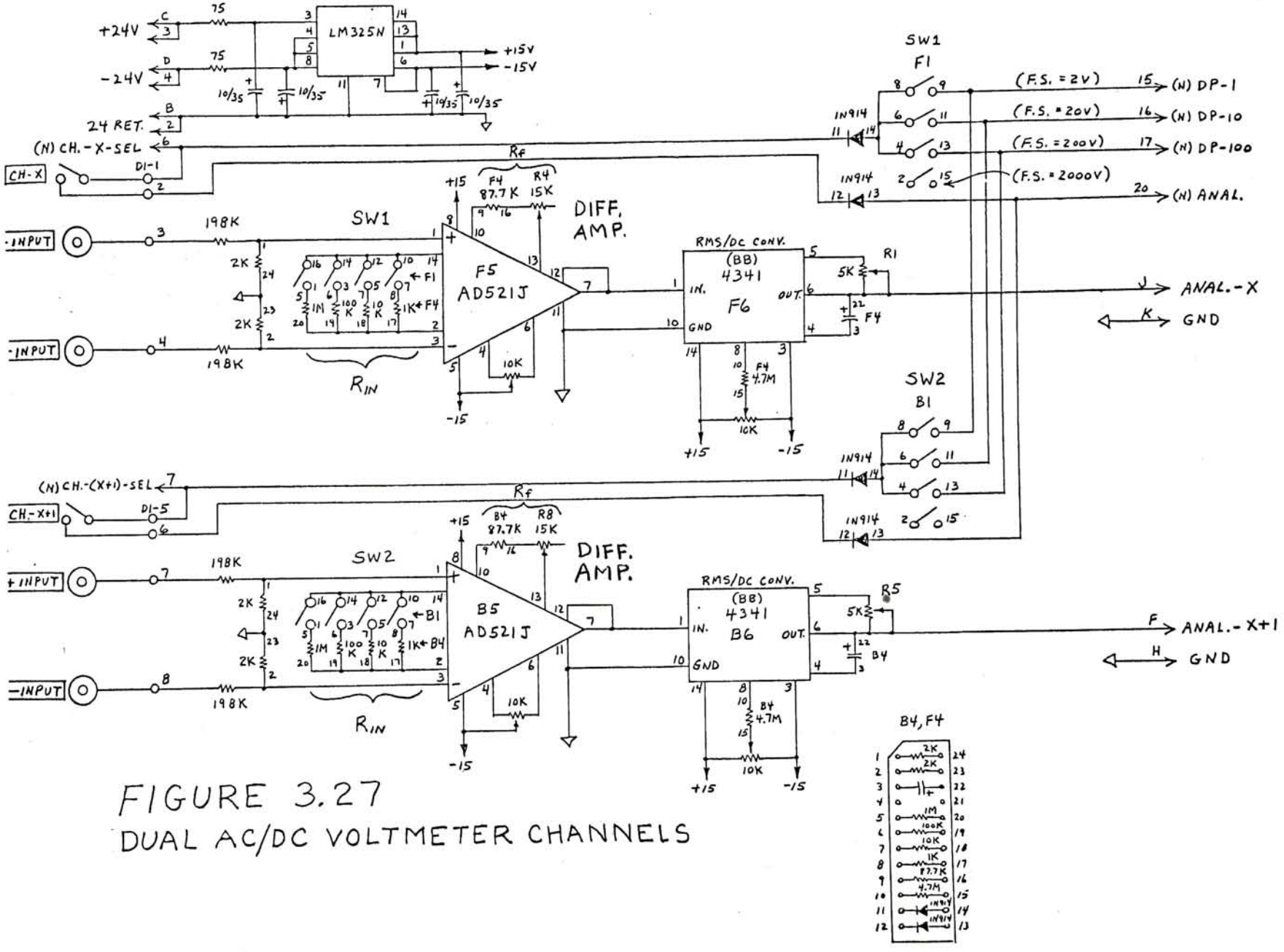


FIGURE 3.27
DUAL AC/DC VOLTMETER CHANNELS

3.2.8 Selection of a Method for BCD to ASCII Conversion and for Transmission of the Floating Decimal Point

All analog and digital data must be converted from BCD code to ASCII code and transmitted to the Line Printer. Additional characters which must be converted to ASCII code for transmission to the Line Printer are: +, -, SPACE, #, $, ., and CR (carriage return). The CR code causes the Line Printer to print the line of data which it received and stored in a Line Buffer Memory. The Printer Line Buffer Memory enables the Synchronous Data Acquisition System (S.D.C.S.) to transmit data from each data channel as it is received and converted to ASCII code, thus eliminating the need to store all 20 channels of data in the S.D.C.S., then transmitting it to the Line Printer after the twentieth channel is processed.

Conversion from BCD to ASCII code is simple, requiring the addition of the four most significant bits of the ASCII code (see Table 3.2). The MSB is a parity bit and is not required, therefore its input at the line printer will be grounded (logic Ø). Since only the circled characters are used in columns 1, 3 and 4, and bit 7 is a logic Ø for these columns, bit 7 can also be tied to ground. Bit 6 is a logic Ø only when a carriage return (CR) code is transmitted to initiate printing, therefore this CR bit can be controlled by the CR function.

TABLE 3.2 MATRIX ASCII CODE

BIT 4	BIT 3	BIT 2	BIT 1		BIT 7	0	0	0	0	1	1	1	1
					BIT 6	0	0	1	1	0	0	1	1
					BIT 5	0	1	0	1	0	1	0	1
0	0	0	0				•	SPACE	ø	@	P	◣	p
0	0	0	1			DC1	!	1	A	Q	a	q	
0	0	1	0				•	"	2	B	R	b	r
0	0	1	1				•	#	3	C	S	c	s
0	1	0	0			EOT	•	$	4	D	T	d	t
0	1	0	1				•	%	5	E	U	e	u
0	1	1	0				•	&	6	F	V	f	v
0	1	1	1				•	'	7	G	W	g	w
1	0	0	0				•	(	8	H	X	h	x
1	0	0	1				•	)	9	I	Y	i	y
1	0	1	0			LF	•	*	:	J	Z	j	z
1	0	1	1				•	+	;	K	[	k	{
1	1	0	0			FF	•	,	<	L	\	l	¦
1	1	0	1			CR	•	-	=	M	]	m	}
1	1	1	0				•	.	>	N	↑	n	~
1	1	1	1				•	/	?	O	←	o	■

96 CHARACTER SET (OPTIONAL)

LEGEND

EOT	END OF TRANSMISSION	CR	CARRIAGE RETURN
LF	LINE FEED	DC1	STANDARD CODE FOR SERIAL PRINT TO PLOT MODE CHANGE
FF	FORM FEED		

NOTE: EMPTY SPACES ARE UNASSIGNED AND IGNORED. *Optional codes for serial print/plot mode change.

The CR code can be transmitted any time after transmission of the last data channel. A convenient time for transmission of the CR code is during channel 21 time. During this period, the first of three reference voltages is converted by the A/D converter. Instead of transmitting the reference voltage, the CR code will be transmitted if printing is required, otherwise a CLEAR signal will be transmitted, causing the print buffer to become initialized.

The print format for time and for data are shown in Table 3.3. Multiplexing is obviously required to perform this task. The task can be broken into two separate design tasks as follows:

a. Transmission of the three data digits and decimal point in the proper sequence. The decimal point (or dollar sign) can be in any one of four positions as shown in Table 3.3.
b. Transmission of time, CR, SPACE, +, -, and the # code.

The more difficult problem is that of transmitting the decimal point (or dollar sign) in the required sequence . . . column 3, 4, 5 or 6 (Table 3.3). Transmission of time, CR, SPACE, +, -, and the # code is a straightforward multiplexing problem and will be designed later.

Before the decimal point problem can be resolved, the entire printing requirement must be defined. The following rules will apply to printing:

TABLE 3.3 PRINT FORMAT FOR TIME AND DATA

	COLUMN NO.					
	1	2	3	4	5	6
TIME (SEC.)	S	D	C	B	.	A
	S	±	C	B	A	.
	S	±	C	B	.	A
ANALOG	S	±	C	.	B	A
(IN-TOLERANCE)	S	±	.	C	B	A
	S	±	C	B	A	$
	S	±	C	B	$	A
	S	±	C	$	B	A
	S	±	$	C	B	A
	#	±	C	B	A	.
DIGITAL	#	±	C	B	.	A
OR	#	±	C	.	B	A
ANALOG	#	±	.	C	B	A
(OUT OF	#	±	C	B	A	$
TOLERANCE)	#	±	C	B	$	A
	#	±	C	$	B	A
	#	±	$	C	B	A

NOTES:

1. A,B,C,D = ANY DIGIT FROM Ø - 9.
2. ± INDICATES THAT A "+" OR "-" IS PRINTED.
3. COLUMN 2 MAY BE A SPACE FOR DIGITAL DATA.

a. Time will always be printed first, followed by the data channels.

b. Data channels will be printed with no spaces due to unused data channels. As an example, if only Channel 20 is used then it will be printed immediately after time (in columns 7-12).

c. If a digital channel has no valid data, then only the decimal point will be transmitted to the printer. A space code will replace the remaining characters.

d. A CR code or a CLEAR signal will be transmitted during the channel 21 period. The CR causes the printer to print the contents of the print buffer. When the CLEAR signal goes true the print buffer is initialized and no printout occurs.

Columns 3 thru 6 (Table 3.3) clearly defines the multiplexing problem. It is a simple task to transmit a "D.P." code or the "$" code, so for the sake of simplification only the "D.P." will be referred to. Note that column 3 can be a C or D.P., column 4 can be a C, B or D.P., column 5 can be an A, B or D.P., and column 6 can be an A or D.P.

Since time, analog data, and digital data are multiplexed to the control panel, data compression logic (analog data only), and to the printer control logic, it may be wise to determine the method of data transfer before a solution to the printer control logic is started. Since three sources of multi-digit data must be transferred to three

locations, a serial approach is generally the best because less I.C.'s and wiring is required to multiplex data serially.

A design solution which appears simple is shown in Figure 3.28-(a). This solution requires the most significant digit (MSD) of the data word to be shifted into the shift register first. Figure 3.28-(b) shows the typical format of the data to be multiplexed. The first character to be transmitted to the printer is the "space" or "#". The next character is the "space", "+", or "-" code. The space is transmitted if the + and - bits are both false. The MSD must be stored and later used to determine if a D.P. or $ code must be transmitted.

Referring to Figure 3.28-(b), the multiplexing sequence of digits C, B and A is dependent upon the location of the decimal point. Columns 3, 4, 5 and 6 of Table 3.3 show that four distinct sequences of the digits and decimal point exist. The multiplexing logic required for these sequences is complex. An example of the timing requirement for the sequence C, (D.P.), B, A is shown in Figure 3.29. For this sequence the counter which is required for generation of the 4-bit multiplex code must be stopped for four

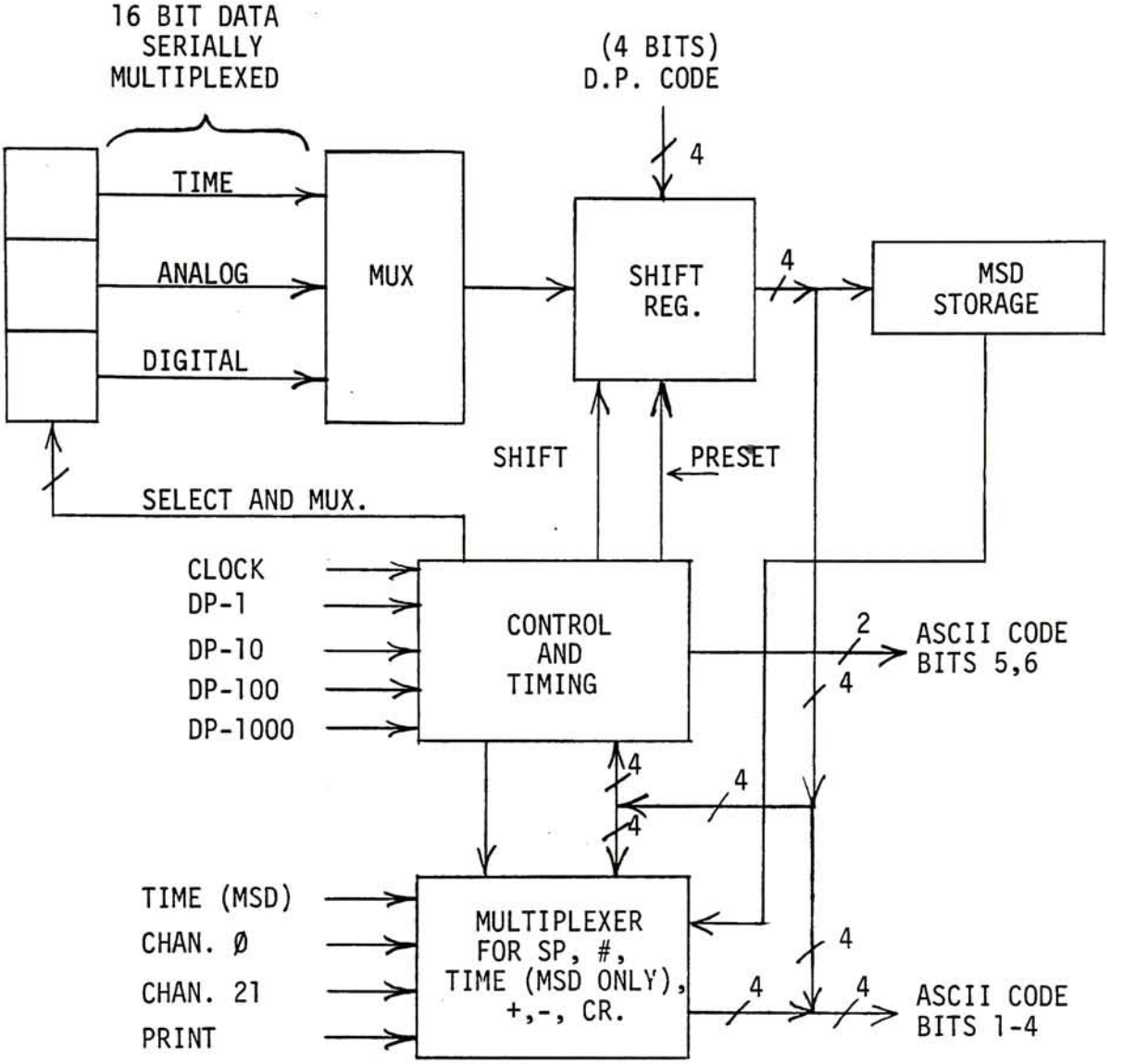


FIGURE 3.28-(a). PRINT MULTIPLEX SOLUTION NO. 1

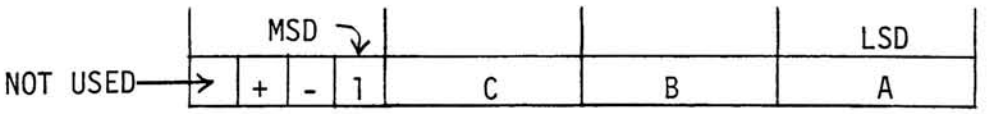


FIGURE 3.28-(b). TYPICAL DATA FORMAT

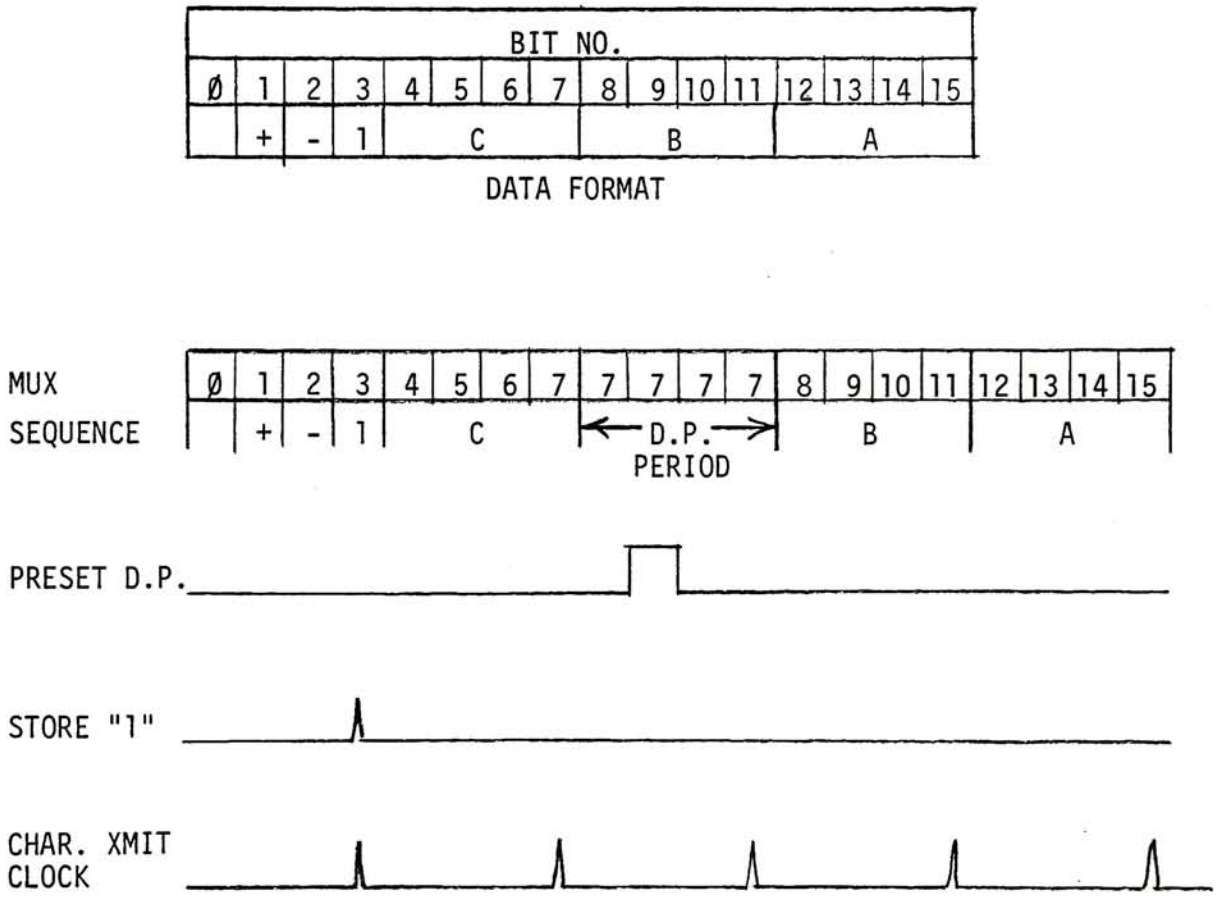


FIGURE 3.29 MULTIPLEX SEQUENCE FOR C, D.P., B, A.

clock pulses during the D.P. period. During this period, the shift pulses to the shift register in Figure 3.28-(a) must be inhibited and the D.P. code must be preset into the shift register. Note the additional timing requirement of the STORE "1" pulse for storage of the MSD, and "character transmit clock" timing (Fig. 3.29). It is obvious that another design approach must be considered.

Some control logic can be shared for the multiplexing requirement of data and time to a display and print register. The multiplex timing used for transfer of 16-bit analog data for the data compression control sub-system (para. 3.2.1) can also be used to multiplex data for the display and print registers.

The second solution which involves shifting of the entire 16 bits of data is shown in Figure 3.30. In this solution tricky timing is replaced by the DIGITAL AND DECIMAL POINT MULTIPLEXER. The "multiplex control" lines for this multiplexer must select four sequences of four digits, each digit consisting of four bits. This results in the multiplexing of 4x4x4 or 64 bits. Eight 8-bit multiplexers (type 4512) are required for this task. The decimal point location which is sent to the "control logic and timing" function (Fig. 3.30) can be used to select the required

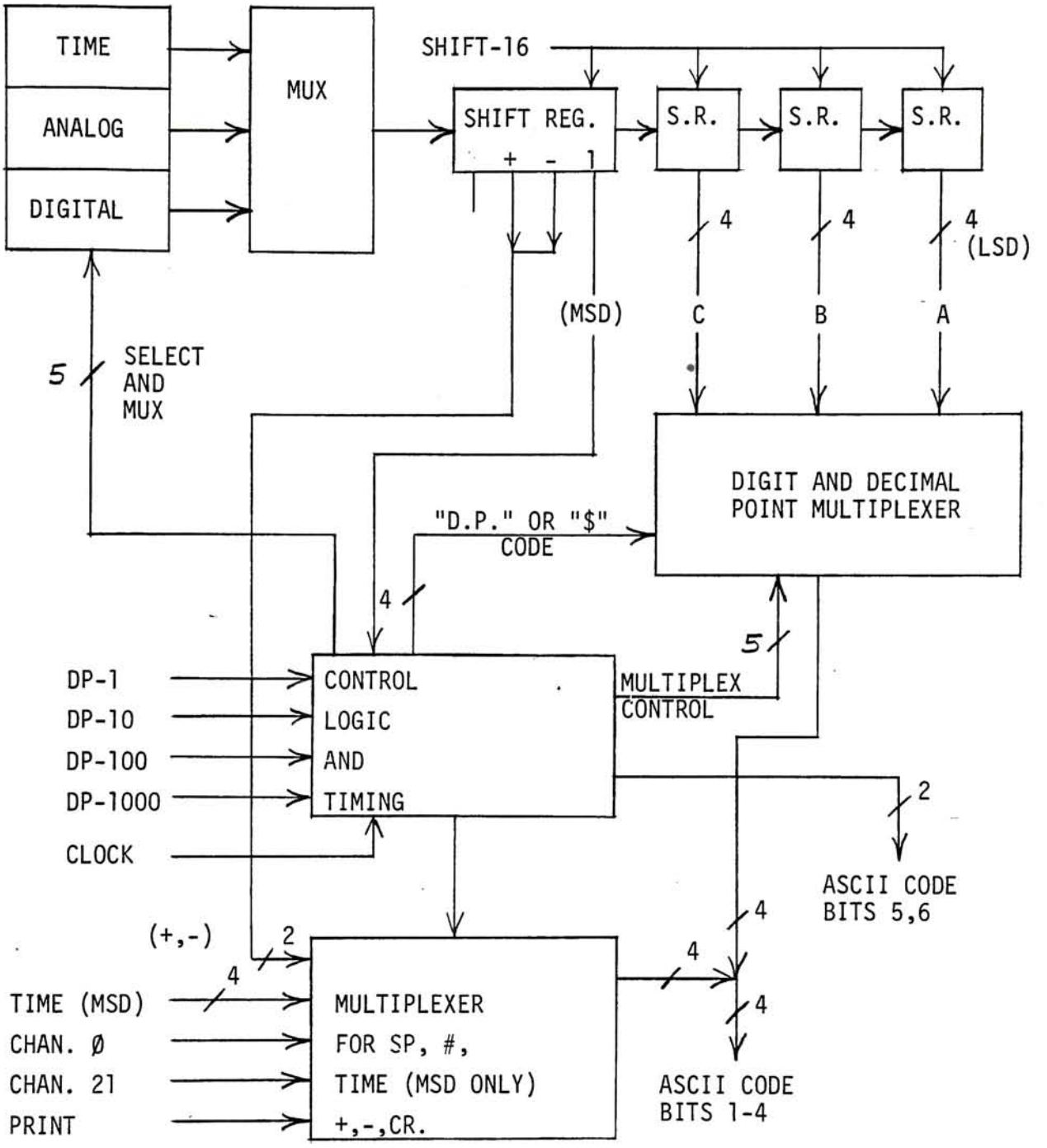


FIGURE 3.30 PRINT MULTIPLEX SOLUTION NO. 2

sequence. This method for print multiplexing is superior to the first solution and will be used for the design solution.

The multiplexing requirement for time (MSD only), CR, SPACE, +, -, and the # code is straightforward and will therefore be covered in the detailed design of the print multiplexer.

4. System Timing Requirements

4.1 Primary System Timing

The primary system timing is defined as that timing which can be used for the timing requirements of all sub-system functions. The frequency range of the timing system must cover the highest and lowest sub-system frequency requirements.

A number of sub-system frequency requirements have already been established and are summarized as follows:

4.1.1 Each data channel is selected for one millisecond.

4.1.2 During an analog data channel select time the following functions must be performed:

a. The analog value (voltage) is multiplexed and allowed to settle. The time allowed for the voltage to settle should be in the range of 10 to 100 microseconds, and depends upon the analog circuitry requirement between the multiplexer output and the A/D converter input. At this time it will be assumed that the 100 microsecond period will be required.

b. The analog value must be converted to digital form by the A/D converter. This conversion time will require as much of the 1.0 millisecond channel select time as possible, and will be determined later.

c. The data compression function requires serial addition, subtraction, compare, and memory update of 16-bit data. If it is assumed that the serial functions are performed at a rate of four microseconds per bit, then each of the four functions can be performed in 64 microseconds for a total time of 256 microseconds.

d. BCD-to-ASCII code conversion and transmission to the line printer is required. At this time the assumption will be made that the required timing can be derived from the data compression timing. No additional time is then required for this function.

e. The BCD data must be transmitted to the display register. This function can also be performed with the data compression timing and can therefore require no additional time.

4.1.3 During a digital channel select time the digital data must be serially multiplexed to the display and print registers. This function can also be performed simultaneously with the data compression function, using the data compression timing.

The data compression function requires the highest frequency, which is 250 KHZ for obtaining a 4 microsecond per bit time. An 8 MHZ crystal oscillator is readily available at Xerox, and is packaged in a 14 pin D.I.P. The basic system timing is in multiples of 10, therefore the 8 MHZ clock will be divided by 8 to obtain a 1 MHZ clock. All lower frequencies will then be derived by decade counters.

Figure 4.1 shows how the 1 MHZ clock is divided-down to obtain all the primary system timing. The 34017 is a decade counter/ decoder. The time period that each decoder output is a logic 1 (high) is indicated above each 34017 divider.

The two primary frequencies are 1 KHZ, which is the data channel select time, and 10 HZ which is the repetition rate for scanning all data channels and for printing. This selection of timing provides all the required timing for the data channel period

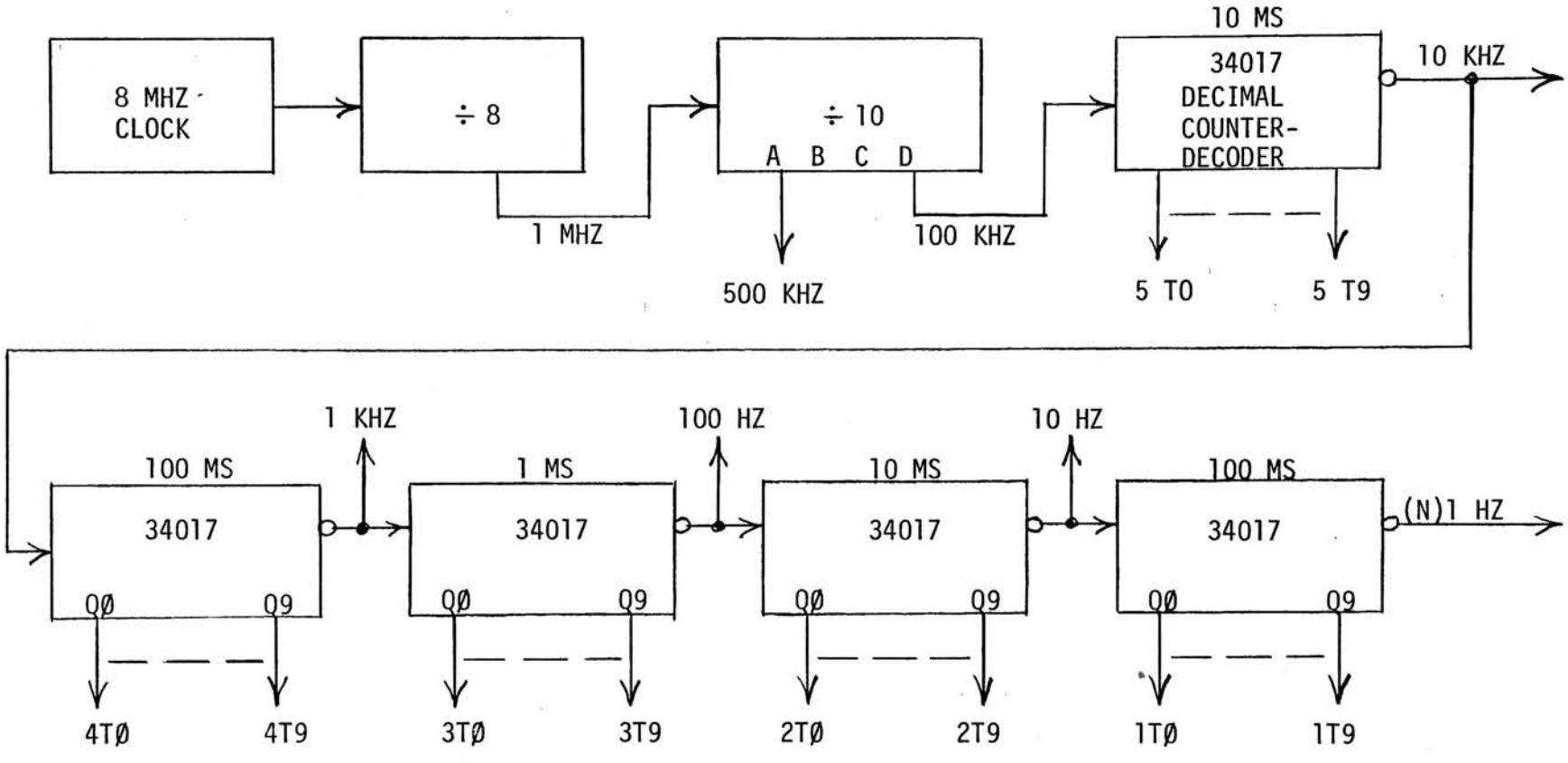


FIGURE 4.1 PRIMARY SYSTEM TIMING

(1 millisecond) timing, data channel scan rate (100 milliseconds) timing, as well as other timing requirements. Note that the "A" output of the first divide-by-10 is 500 KHZ. This value will be used for the data compression logic instead of 250 KHZ.

4.2 Secondary System Timing

The secondary system timing requirements are numerous. Only the general timing requirements will be developed here. All other secondary or sub-system timing will be developed when each sub-system is designed.

4.2.1 Data Channel Select Timing

The data channel select timing includes the binary code required for multiplexing data and the generation of a single channel select signal for each of the 20 data channels, the time channel, and the three voltage reference channels.

The 1 KHZ signal shown in Figure 4.1 can be used to generate the 5-bit binary code which is required for generating binary counts Ø thru 23. Since all channels are scanned once every 100 milliseconds, a 7-bit binary counter is required. This counter must then count from Ø to 99 and must also be synchronous with the 100 millisecond time period of the 10 outputs of the last decade counter in Figure 4.1. This is accomplished with the logic shown in Figure 4.2. The SET Ø F/F is required to obtain a synchronous reset pulse [(P) SET Ø] to the 4024 7-stage binary counter at the beginning of every 100 millisecond period. This reset actually occurs when the counter starts count 100. The "5T1" signal is a convenient reset time because it occurs only 10 microseconds after the set Ø F/F gets set by the 10 HZ signal.

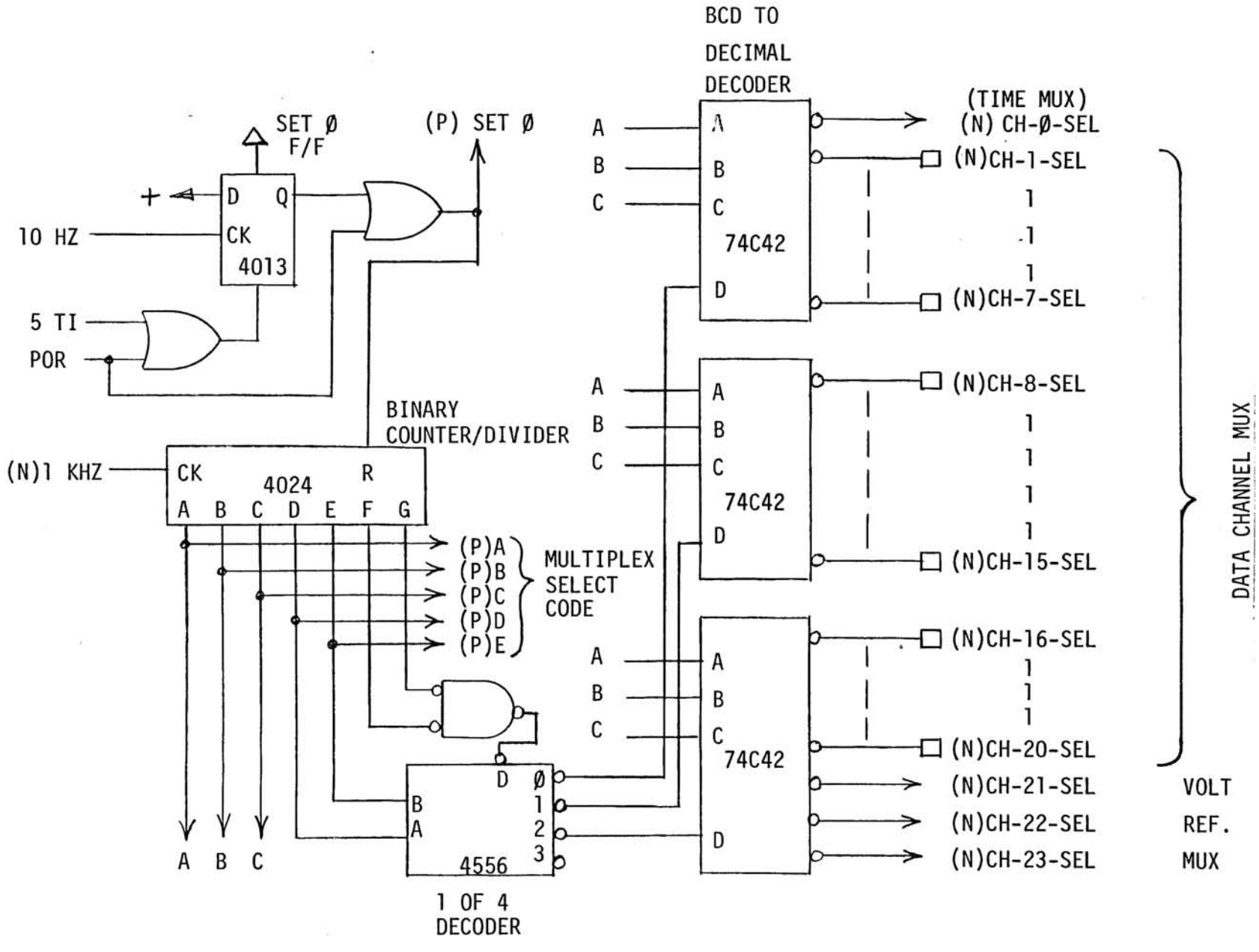


FIGURE 4.2 MULTIPLEXED AND ENCODED CHANNEL SELECT

The "5T1" signal is generated in the primary system timing logic shown in Figure 4.1.

The counter outputs (P)A thru (P)E is the required channel number code which will be used for various functions. One function is shown in Figure 4.2. Here, three 74C42 BCD to decimal decoders are used to demultiplex the channel select signals Ø thru 23. The 4556 is a dual 1-of-4 decoder/ demultiplexer and selects the 74C42's as shown.

Another set of three 74C42 IC's are required to obtain the CHANNEL SET function for each of the 20 data channels. This function is described in paragraph 3.2.7, page 62. The enable input ($\overline{E}$) of the 4556 is a data channel reset signal which occurs after analog and digital data is transmitted to the main logic. This signal can be derived by ANDing 4T9 and 5T8 signals. The resultant signal will then occur 10 microseconds before the end of each channel select time.

4.2.2 Digital Data Channel Clock/Counter

The digital data interface requires a 1 KHZ clock and a reference counter for resynchronization as described in paragraph 3.2.7, page 62. The existing 1 KHZ signal can be used with three decade counters to generate the required function. To guarantee synchronization of this counter with the system, it is necessary to reset it at the beginning of each second (count .ØØØ).

5. Sub-system Design

This section will cover the design of each sub-system. The more challenging or interesting sub-systems will be covered in greater detail than those sub-systems which involve straightforward design.

5.1 Data Channel Monitor Control

The data channel monitor control is accomplished on the control panel and includes data, channel number selection, data tolerance selection, the displayed value of the selected data channel, and the logic required to multiplex the display information to the control panel board.

The control panel board is mounted behind the control panel and contains 8 LED digit displays, the sign display, 12 LED indicators, the indicator demultiplexing logic, and LED drivers. A separate +5V power supply is used for the control panel board to reduce noise on the system +5V supply.

The selection of the data channel selection sub-system design was determined in paragraph 3.2.3, and is shown in Figure 3.13, page 44. An integral part of this system is the data tolerance memory sub-system which is selected and described in paragraph 3.2.4, page 45. The solution for the memory tolerance sub-system is shown in Figure 3.14, page 47.

Integration of Figure 3.13 and 3.14 produces the functional block diagram shown in Figure 5.1. It can be seen that the channel compare function is required primarily for the tolerance memory function. The channel compare is also used to store the data value of the monitored data channel in the data monitor register.

5.1.1 Data Channel Number Selection

The design required for selection of the data channel number

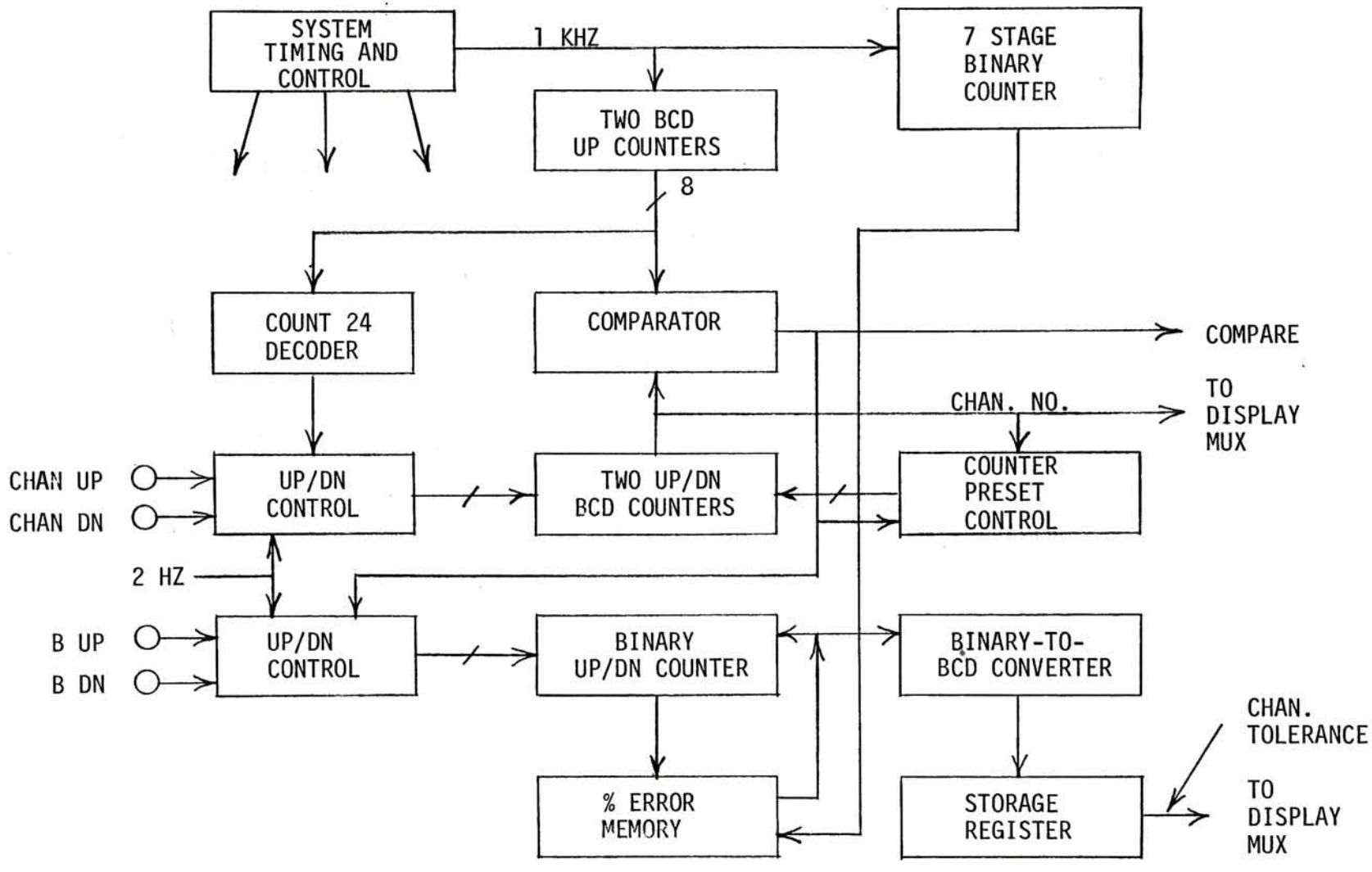


FIGURE 5.1 BLOCK DIAGRAM OF CHANNEL NUMBER SELECTION AND CHANNEL TOLERANCE MEMORY CONTROL.

is straightforward, requiring only two UP/DOWN BCD counters, UP/DOWN CONTROL, and COUNTER PRESET CONTROL as shown in Figure 5.1. When the CHAN. UP or CHAN. DN (down) inputs are activated, the counter increments (or decrements) at a rate of two counts per second. This is accomplished during count 24, which is after all valid channel numbers have been compared.

The control function of the COUNTER PRESET CONTROL is that of presetting the counter to ØØ when it increments to count 24 (23 is max. count) or to count 23 when the counter decrements from ØØ to 99.

The detailed design solution for this sub-system is shown in Figure 5.2. The middle section of the schematic shows the data channel control logic, and includes the IC's in locations G3, G4, N1, M1 and associated gates. Note that the COMPARE signal from IC-H3, pin 6 is tied to J2, pin 11 (located above F/F N1). When the 2 BCD UP COUNTERS (location G2) reach count 24 the gates GØ, J5, and D2 decode this count, producing a high level at input pin J2-12. Pulse 4T3 (at pin J2-13) causes output J2-10 to go high and reset flip flop N1 at pin 8. This action results in counters G3 and G4 to become preset to count Ø from output M1, pin 10.

When counters G3 and G4 decrement from count ØØ to 99, counter G3, pin 2 goes high and resets F/F N1 at pin 6. N1 pin 1 is tied to the proper data inputs of G3 and G4 which causes them to become preset to count 23.

The UP/DN CONTROL function (Fig. 5.1) is straightforward and will therefore not be explained. The origin of the (P) CHAN UP and (P) CHAN DN signals shown in Figure 5.2 will be

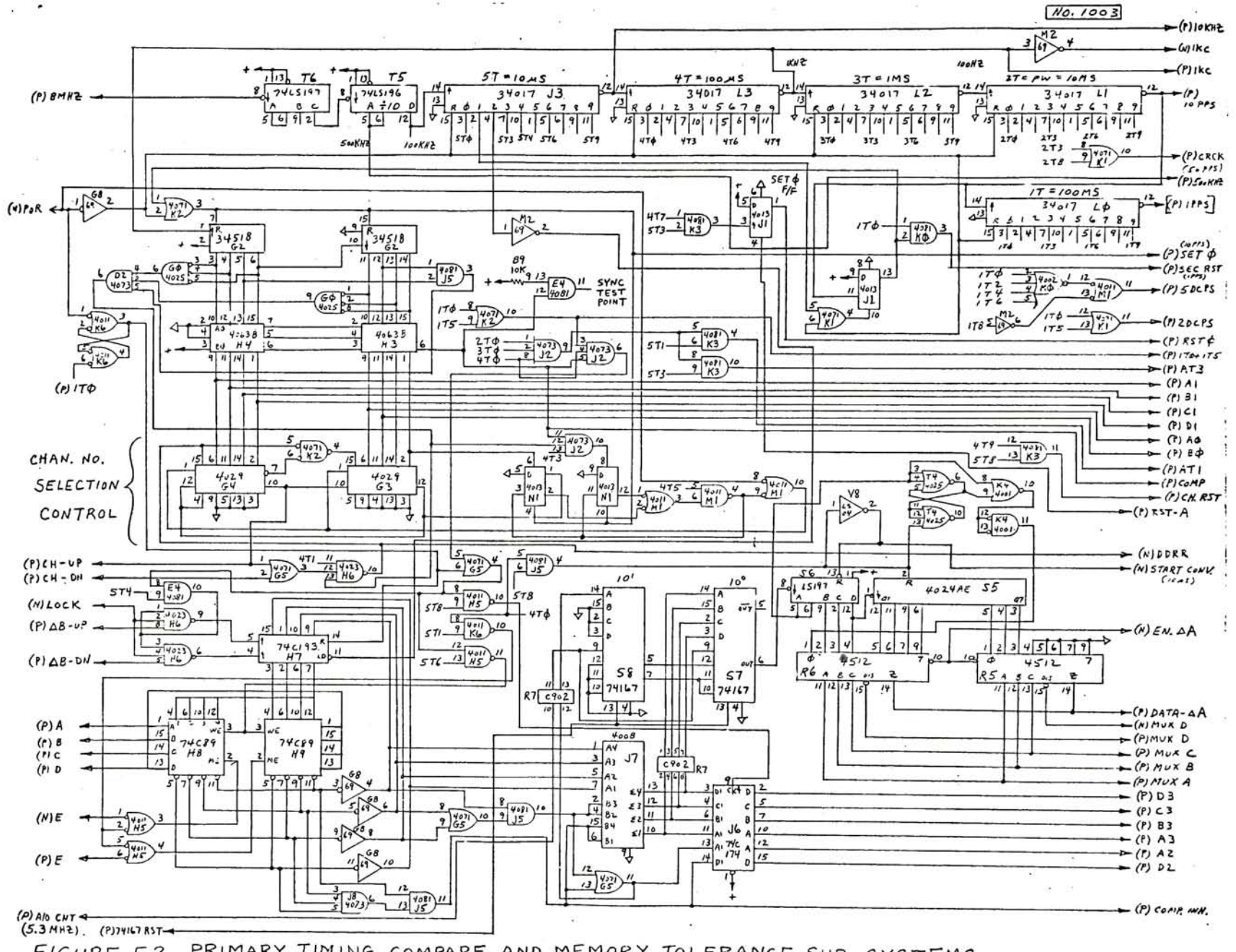


FIGURE 5.2 PRIMARY TIMING, COMPARE, AND MEMORY TOLERANCE SUB-SYSTEMS

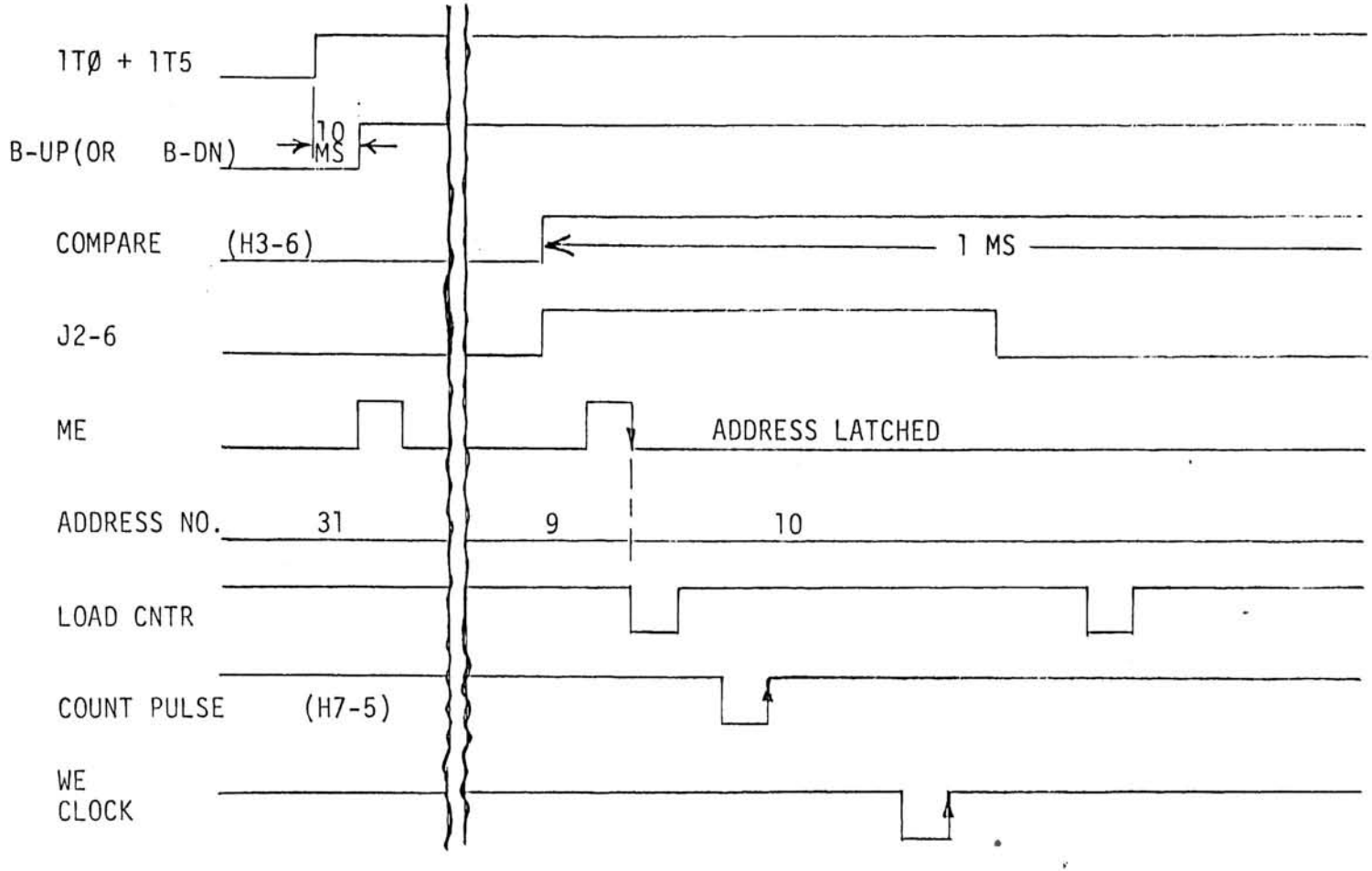
shown later when the "miscellaneous" system functions are designed.

5.1.2 Data Tolerance Memory Design

The detailed design solution for the data tolerance memory is shown in the bottom-left side of Figure 5.2. The two 74C89 16 word x 4 bit memories (location H8, H9) store the channel tolerance for each of the 20 data channels. The memory is addressed by a 7-stage binary counter which is synchronized to the two BCD counters in location G2.

The timing requirements for the tolerance memory are shown in Figure 5.3. This timing diagram shows the signal "1TØ + 1T5" which is obtained by logic ORING signals 1TØ and 1T5 which originated in Figure 5.2, location LØ-3 and LØ-1. If the operator actuates the UP switch then signal Δ B-UP goes positive 10 microseconds after the lead edge of signal "1TØ + 1T5" and stays high for 100 milliseconds. During this 100 millisecond period the COMPARE signal will go positive for 1 millisecond during the time that the monitored channel number is selected. During this time counter G2 is equal to counter G3, G4, and output H3-6 is high. Note that "H3-6" means "location H3, pin 6." The COMPARE signal is tied to gate J2-5 and ANDED with 4TØ and K2-10 to obtain J2-6 as shown in the timing diagram. This signal is used to enable the (P) ΔB-UP, (P)ΔB-DN, WE, and CLOCK signals shown in the timing diagram.

The Memory Enable (ME) signal is required to latch each data channel number into the memory address select register which is located in the 74C89. Immediately after the ME signal, a LOAD CNTR signal loads the contents of the selected



FUNCTION TABLE FOR 74C89

ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	WRITE	COMPLEMENT OF DATA INPUTS
L	H	READ	" " SELECTED WORD
H	L	INHIBIT STORAGE	" " DATA INPUTS
H	H	DO NOTHING	HIGH

FIGURE 5.3 TOLERANCE MEMORY TIMING

memory address into the UP/DN counter in location H7. For this example, the △B-UP switch has been activated, so the COUNT PULSE at H7-5 causes the counter to increment. This is followed by a WRITE ENABLE (WE) pulse to the selected 74C89 which causes the incremented count to be stored in memory. Finally, the CLOCK pulse stores the new value (after conversion to BCD) in display register J6.

The function table in Figure 5.3 shows how the 74C89 operates. The ME signal is normally low and the WE signal is normally high, which results in the 74C89 being normally in the read mode. This is required to obtain the tolerance readout of each data channel during A/D conversion and apply it to the BCD rate multipliers (location S7 and S8). The operation of the BCD rate multipliers will be discussed in paragraph 5.4.7.

When power is turned on a Power On Reset (POR) signal is generated for approximately 100 milliseconds. This signal is shown on the top left corner of Figure 5.2 and is used to set flip flop K6. During the time that the K6 flip flop is set, counter H7 is reset, resulting in ØØ stored in all memory locations.

IC J7 is a 4-bit binary adder and is required to convert binary numbers greater than 9 to a BCD digit by adding 6 to the B inputs. When this is done, a 1 must be stored in the tens register of J6.

Gates J8 and J5 are used to decode ØØ and produce a 99 for storage in J6 and a (P) COMP. INH. signal for use in the data compression sub-system.

5.1.3 Control Panel Data Multiplexer

The schematic in Figure 5.4 shows the detailed design solution for multiplexing channel number, channel tolerance, and channel data to the control panel. The four IC's shown in the top right corner are not part of this sub-system.

The Data Monitor Register and associated logic gates are required to select and store time or data from channels Ø thru 23. Note that the "(P) COMP." is used to enable the 16 shift pulses ["(P)SHIFT-16] at gate D2, causing the monitored data to shift into the data monitor register at input F2-7. The remainder of the gating is required to shift time and converted analog data into the register two times per second (with 1TØ and 1T5) or to shift digital data into the register with "(N) DIG. VAL'." any time that valid digital data exists on the monitored digital channel. The four 1 of 8 multiplexers (74C151) are required to sequentially select the 8 BCD digits and to transmit them to a demultiplexer on the control panel board (see Figure 3.11, page 41).

A 10 KHz signal is used to increment the 4-bit binary counter shown in Figure 5.4, location H2. The three most significant digits of this counter are used to multiplex the eight BCD digits to the control panel. These three digits are also transmitted to the control panel board for use in the demultiplexer.

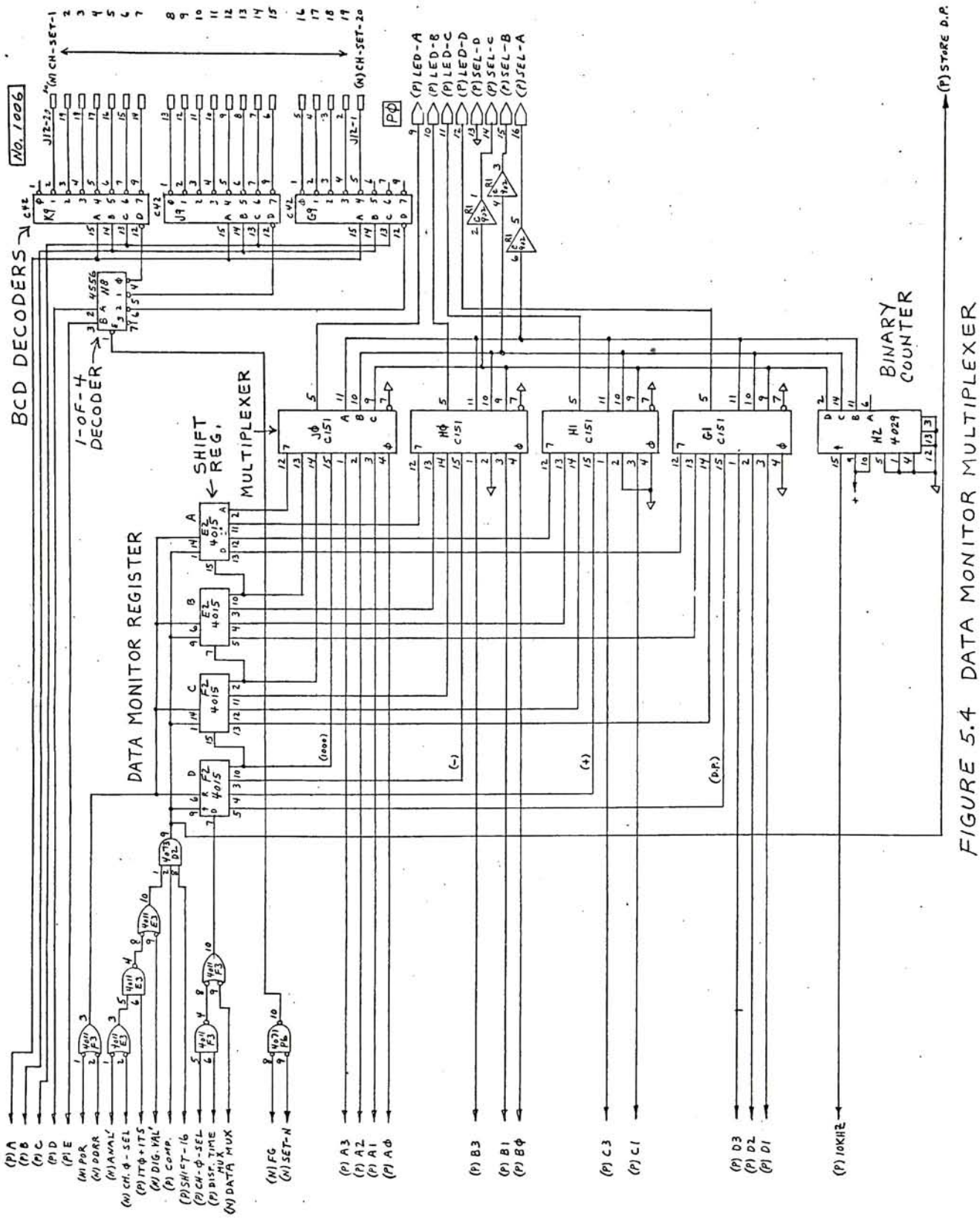


FIGURE 5.4 DATA MONITOR MULTIPLEXER

5.2 Data Compression Rate and Sample Rate Selection

The sub-system design for the data compression rate and sample rate selection logic is shown in Figure 5.5. The counters located at the top of Figure 5.5 are required to obtain pulse rates of 1 second, 10 seconds, 1 minute and 10 minutes as shown. Each of these pulse rates is tied to the clock of a D-type flip flop in locations R2 and R3. When the D input of a flip flop goes high, the $\overline{Q}$ output (pin 2 or 12) goes low at the beginning of 1TØ. ITØ is the first of ten 100 millisecond intervals (see Fig. 5.2, location LØ). The flip flop is then reset after the termination of 1TØ by signal (P) 1T1. All four flip flop outputs are OR'ed at gate R4-1, generating a (P) SAMPLE pulse for 100 milliseconds at the selected sample rate.

The two identical rate selection functions for sample rate and compression rate selection are shown on the left half of Figure 5.5. This circuit was developed and selected in paragraph 3.2.5 and is illustrated in Figure 3.18. The AND gates in location S3 (Fig. 5.5) are required to select the proper 100 millisecond intervals; (P) 5DCPS, (P) 2DCPS, (P) 1DCPS, or continuous DCPS. DCPS is "Data Compression Pulses per Second." The derivation of these signals is shown in Figure 5.2.

The line buffers in locations TØ and SØ transmit the selected sample rates to the control panel board to turn on the corresponding LED sample rate indicators.

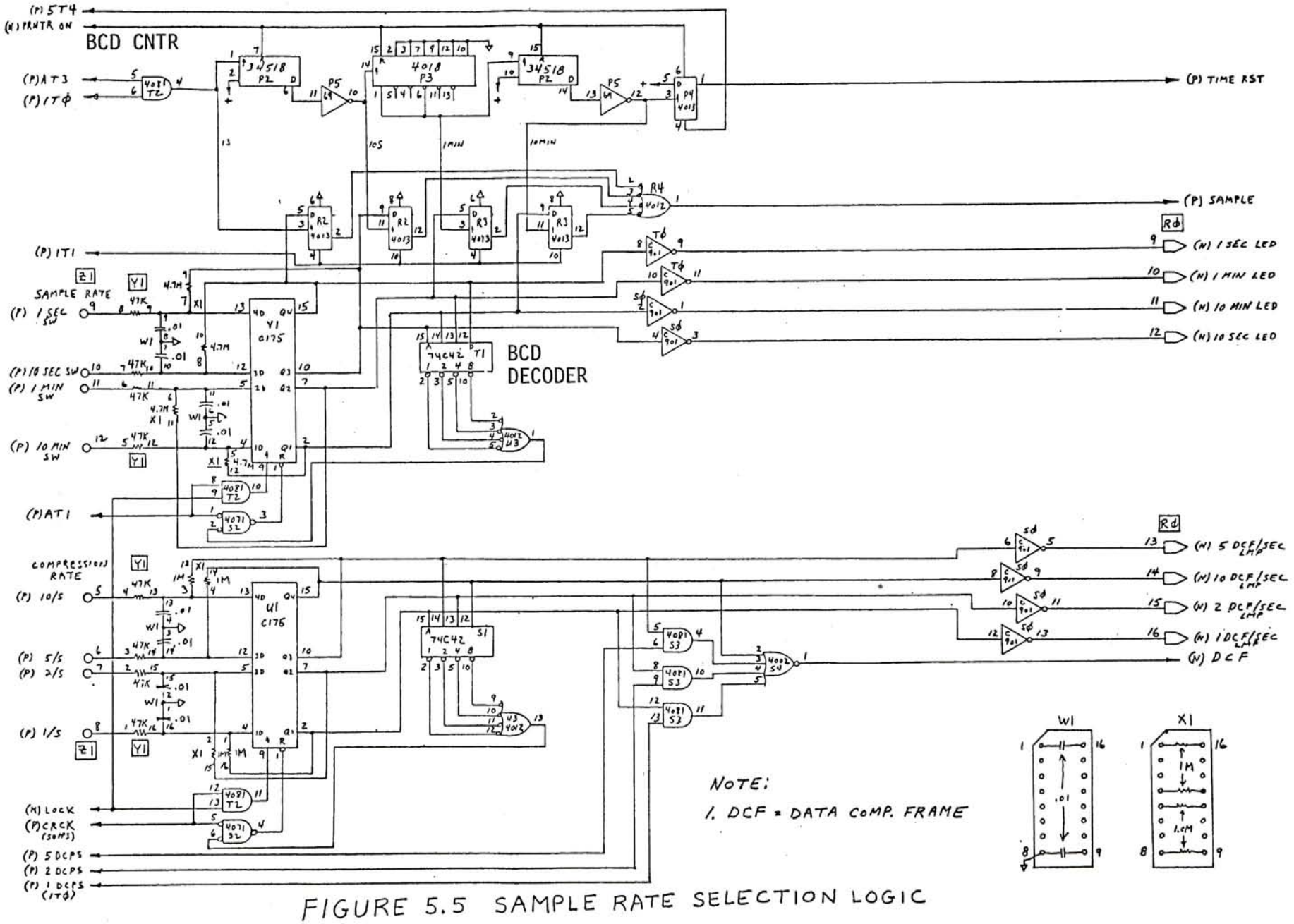


FIGURE 5.5 SAMPLE RATE SELECTION LOGIC

5.3 Data Compression Sub-System

The digital solution for performing data compression is one which incorporates a serial technique of addition, subtraction, compare, and storage of binary coded data. This digital method has been selected because it requires the minimum number of I.C.'s, conforms to the general system serial data flow, and is also the easiest type to build and debug.

A functional block diagram of upper/lower limit detection is illustrated in Figure 5.6. Data stored in memory will be designated as "B" and data deviation (percentage of B) will be designated as "ΔB". New data will be designated as "A" and new data deviation (percent of A) will be designated as "ΔA".

5.3.1 Limit Compare Method

Limit compare consists of a sequence of three functions as shown in Figure 5.7-d. The first function (STEP 1) is serial generation and storage of the binary value of the upper and lower limits for the selected data channel. The second function (STEP 2) is serial comparison of new data from the selected channel with the stored limits. The third function (STEP 3 and 4) is serial storage of A and ΔA respectively if the new data (A) exceeds the limits of B $\pm$ ΔB.

Figure 5.6 shows the basic functions needed to perform limit compare. First, the B and ΔB memory must be initialized by storing all analog data (B) and data deviation (ΔB) for a maximum of 20 data channels. On succeeding data frames the following steps are taken (refer to Fig. 5.6):

Data values B and ΔB are read from memory for the selected channel, serially added to obtain the upper (B + ΔB) and lower (B - ΔB) limits, and stored in the temporary storage memory. Next, the upper and lower limits are serially compared with A to determine if A exceeded either limit. Finally, if either limit is exceeded then B and ΔB is replaced by A and ΔA.

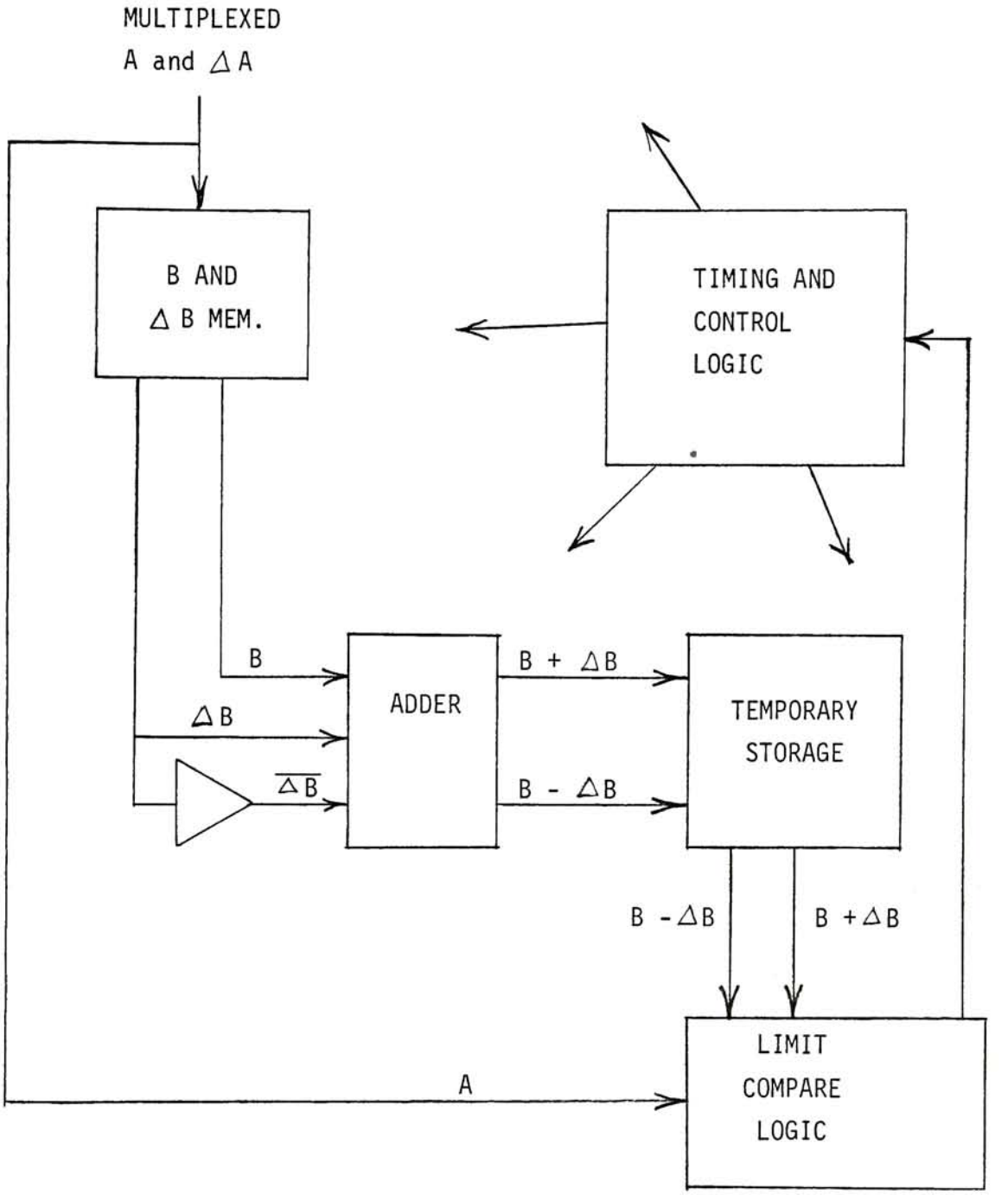
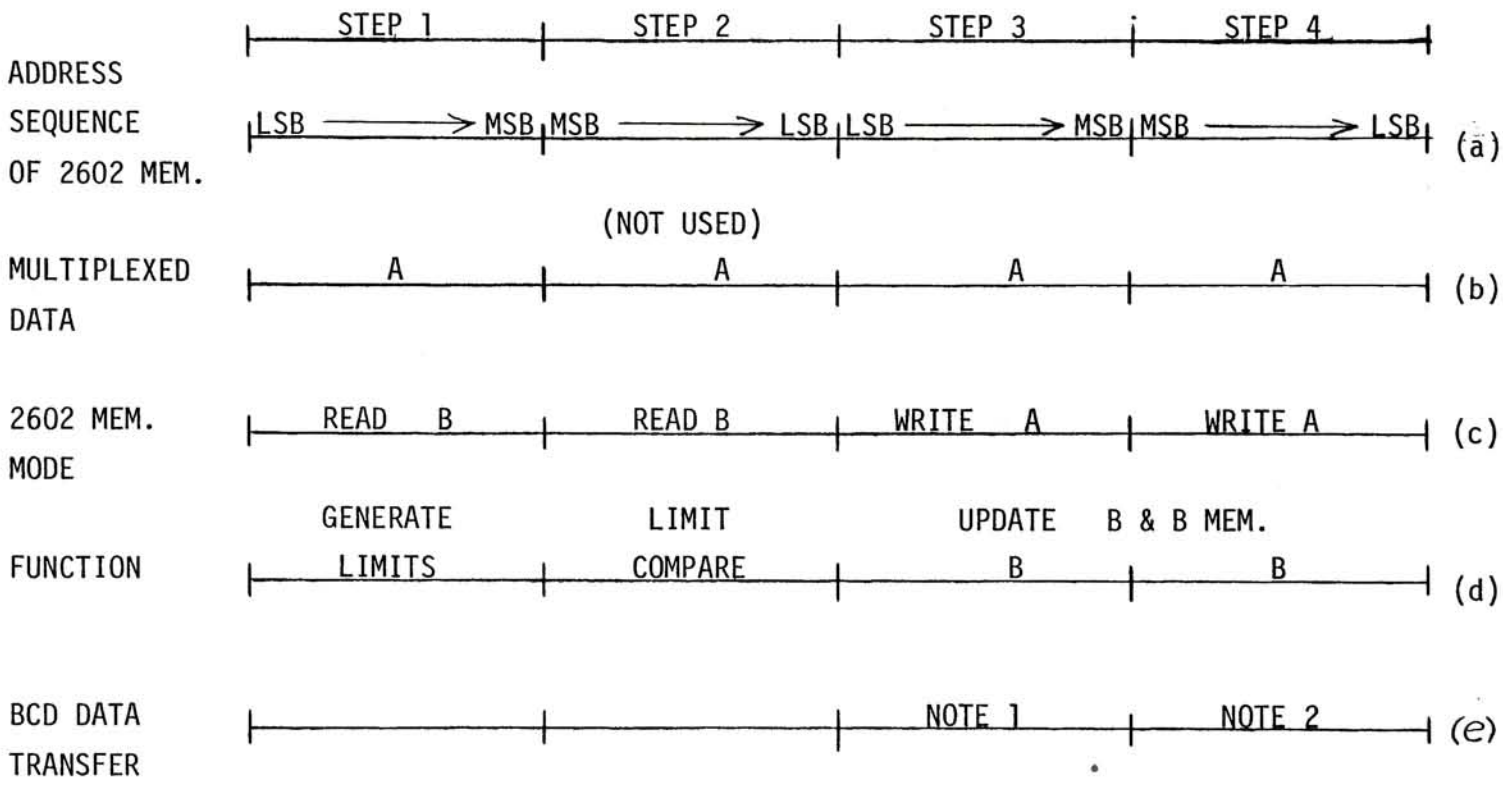


FIGURE 5.6 BASIC LIMIT COMPARE FUNCTIONS



NOTES:

1. ANALOG OR DIGITAL BCD DATA IS SERIALLY TRANSFERRED TO INTERNAL DISPLAY AND PRINT REGISTERS.
2. BCD DATA IN PRINT REGISTER IS CONVERTED TO ASCII CODE AND TRANSMITTED TO THE PRINTER BUFFER.

FIGURE 5.7 LIMIT COMPARE STEPS

Figure 5.8 is an expansion of Figure 5.6, showing how A and ΔA are obtained and how $A - \Delta B$ is obtained. Note that $A - \Delta B = A + \overline{\Delta B} + 1$.

The first function would normally be accomplished by comparing new data (A) with the upper and lower limits of the old data (B) and a selected percentage of the old data (ΔB) as shown in the following equation:

$$B - \Delta B \leq A \leq B + \Delta B \qquad \text{(Eq. 5-1)}$$

All the data values (B) and data deviations (ΔB) can easily be stored in one 1024 Bit memory chip. If 16 bits are assigned to B and ΔB then the total storage requirement is: (No. of Channels) (B + ΔB) (16 Bits) = (20) (2) (16) = 640 BITS

The ideal I.C. for this storage requirement is a 320-word by 2-bit static RAM. Unfortunately, no such I.C. exists. A 256-word by 4-bit memory exists but either two I.C.'s must be used or one I.C. with input demultiplexing and output multiplexing. A second (and better) choice would be the use of a 1024-word by 1-bit memory.

Using one I.C. for storage of B and ΔB means that equation 5.1 cannot be used in its present form since B and ΔB cannot be obtained simultaneously. Equation 5.1 can be modified as follows:

$$B - \Delta B + (-A-B) \leq A + (-A-B) \leq B + \Delta B + (-A-B)$$

Reducing: $-A - \Delta B \leq -B \leq -A + \Delta B$

$$\text{or } A + \Delta B \geq B \geq A - \Delta B$$

$$\text{or } A - \Delta B \leq B \leq A + \Delta B \qquad \text{(Eq. 5-2)}$$

Equation 5.2 can be used with B and ΔB stored in a 2602 [7] RAM and data A stored in an external register as shown in Figure 5.8.

(7) Signetics, Digital-Linear-MOS Data Book, p. 7-121.

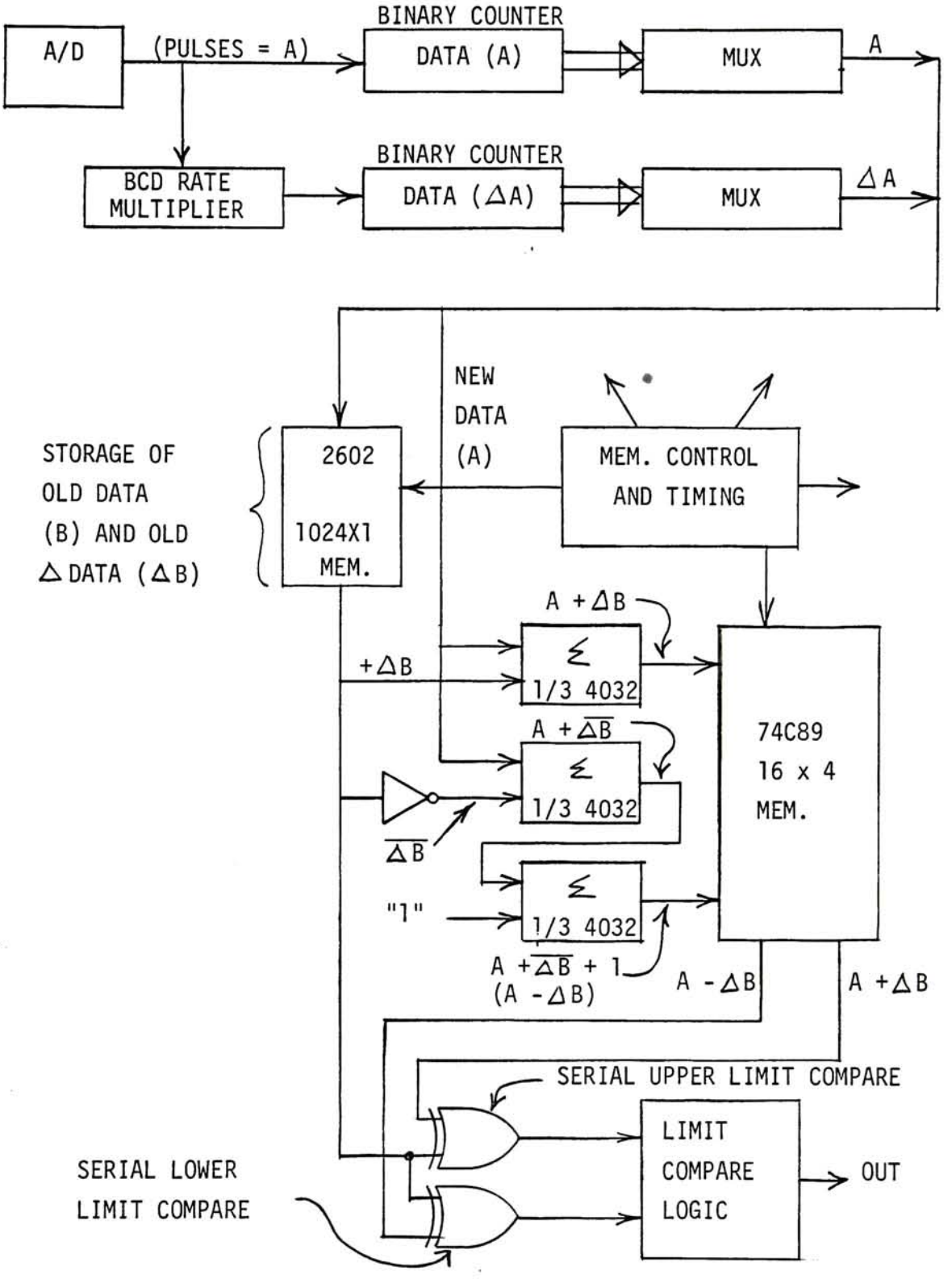


FIGURE 5.8 FUNCTIONAL BLOCK DIAGRAM OF UPPER/LOWER LIMIT DETECTION

5.3.2 Developing the Upper and Lower Limits

Serial summation of A $+\Delta B$ is accomplished with RCA's CMOS I.C. type 4032A which is a Triple Serial Adder. (See Fig. 5.9). The value A $-\Delta B$ must be obtained by summing A with the two's complement of ΔB as shown in the following equation:

$$A - \Delta B = A + \overline{\Delta B} + 1 \qquad \text{(Eq. 5-3)}$$

The remaining two adders of the 4032A can be connected as shown in Fig. 5.9 to produce the summation of $(A + \overline{\Delta B}) + 1$. The "+1" input is a logic 1 only during the first clock pulse. The timing diagram in Fig. 5.9 illustrates how the adder is reset before the summation of $\overline{\Delta B} + 1$. The final timing is dependent on timing requirements for the complete limit compare logic and will be determined later in this section.

5.3.3 Serial Comparison

The second function consists of performing a serial comparison of data B with the newly stored upper and lower limits in accordance with Eq. 5.2. The comparison must be made serially, starting with the MSB and sequentially progressing to the LSB. Table 5.1 shows five compare conditions. Table 5.1 - (a), (b), and (c) shows data value B inside, above, and below the upper/lower limits respectively. Note that in Fig. 5.1 - (a) the value of B compared larger than the value of A $-\Delta B$ at bit b5. Likewise, B compared lower than A $+\Delta B$ at bit b3. These two comparisons resulted from value B being at binary 1 in the first compare difference and a binary Ø in the second compare difference. It is obvious that whenever the value B is within the upper/lower limits, that the first B compare bits will be different.

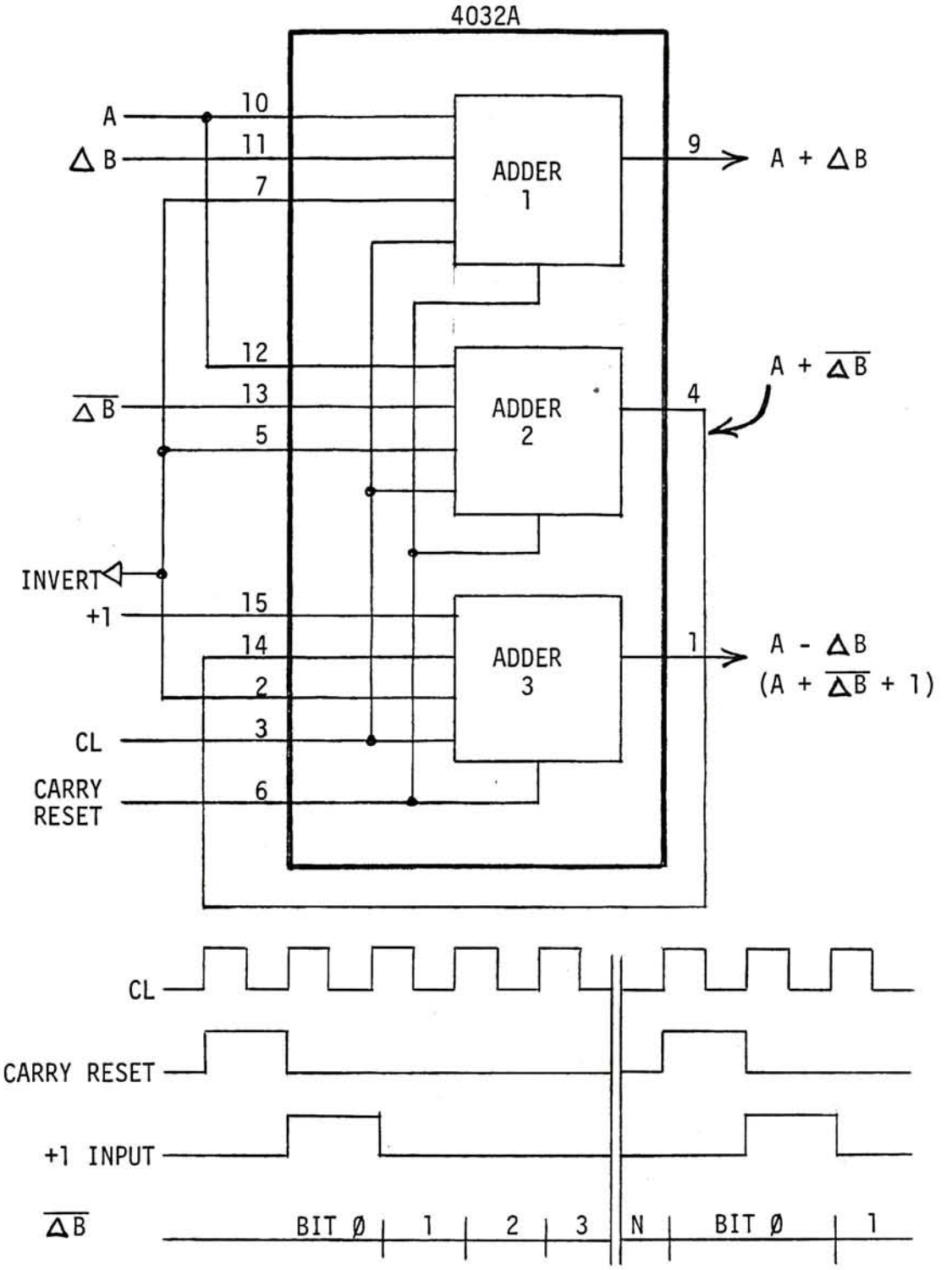


FIGURE 5.9 SERIAL ADDER AND TIMING

	MSB	BINARY VALUE					LSB	
	b6	b5	b4	b3	b2	b1	bØ	
A + ΔB = 110	1	1	0	1	1	1	0	
B = 100	1	1	0	0	1	0	0	(a)
A - ΔB = 90	1	0	1	1	0	1	0	
A + ΔB = 110	1	1	0	1	1	1	0	
B = 114	1	1	1	0	0	1	0	(b)
A - ΔB = 90	1	0	1	1	0	1	0	
A + ΔB = 110	1	1	0	1	1	1	0	
B = 88	1	0	1	1	0	0	0	(c)
A - ΔB = 90	1	0	1	1	0	1	0	
A + ΔB = 110	1	1	0	1	1	1	0	
B = 110	1	1	0	1	1	1	0	(d)
A - ΔB = 90	1	0	1	1	0	1	0	
A + ΔB = 110	1	1	0	1	1	1	0	
B = 90	1	0	1	1	0	1	0	(e)
A - ΔB = 90	1	0	1	1	0	1	0	

TABLE 5.1 FIVE COMPARE CONDITIONS

When the first compare difference values of Table 5-1-(b) and (c) are found, as indicated by the circled bits, it is seen that both bits of value B are equal when the upper or lower limit is exceeded. This basic observation leads to the conclusion that when the first compare difference values of B are equal, then B has exceeded an upper or lower limit.

Note that Table 5.1-(d) and (e) shows a unique condition which occurs only when B is equal to the upper or lower limit. In each case only one compare difference is detected instead of two.

The logic shown in Fig. 5.10 is designed to take this unique condition into account by offering a choice of resets (RST A or RST B) for initalizing F/F-2 and F/F-3. Selection of RST A causes output H to go true if B is equal to the upper or lower limit. Selection of RST B causes output H to go true only if B is greater than A $+\Delta B$ or less than A $-\Delta B$. This operation will be explained later with Fig. 5.10 and the timing diagrams in Fig. 5.11.

The circuit shown in Fig. 5.10 operates as follows: all four flip-flops are first initialized with RST C and RST A or RST B. For this case assume that RST A is used. All four flip-flops are then initialized as shown in Fig. 5.11. Also, assume that the values of A $+\Delta B$, A $-\Delta B$, and B are as shown in Table 5.1 - (c).

When A $+\Delta B \neq B$ then output C of the exclusive - OR gate (A1) goes true (logic 1). This occurs the first time for bit b5 as shown in Fig. 5.11. The trailing edge of the strobe pulse (D) sets F/F-1 during b5 causing F to become

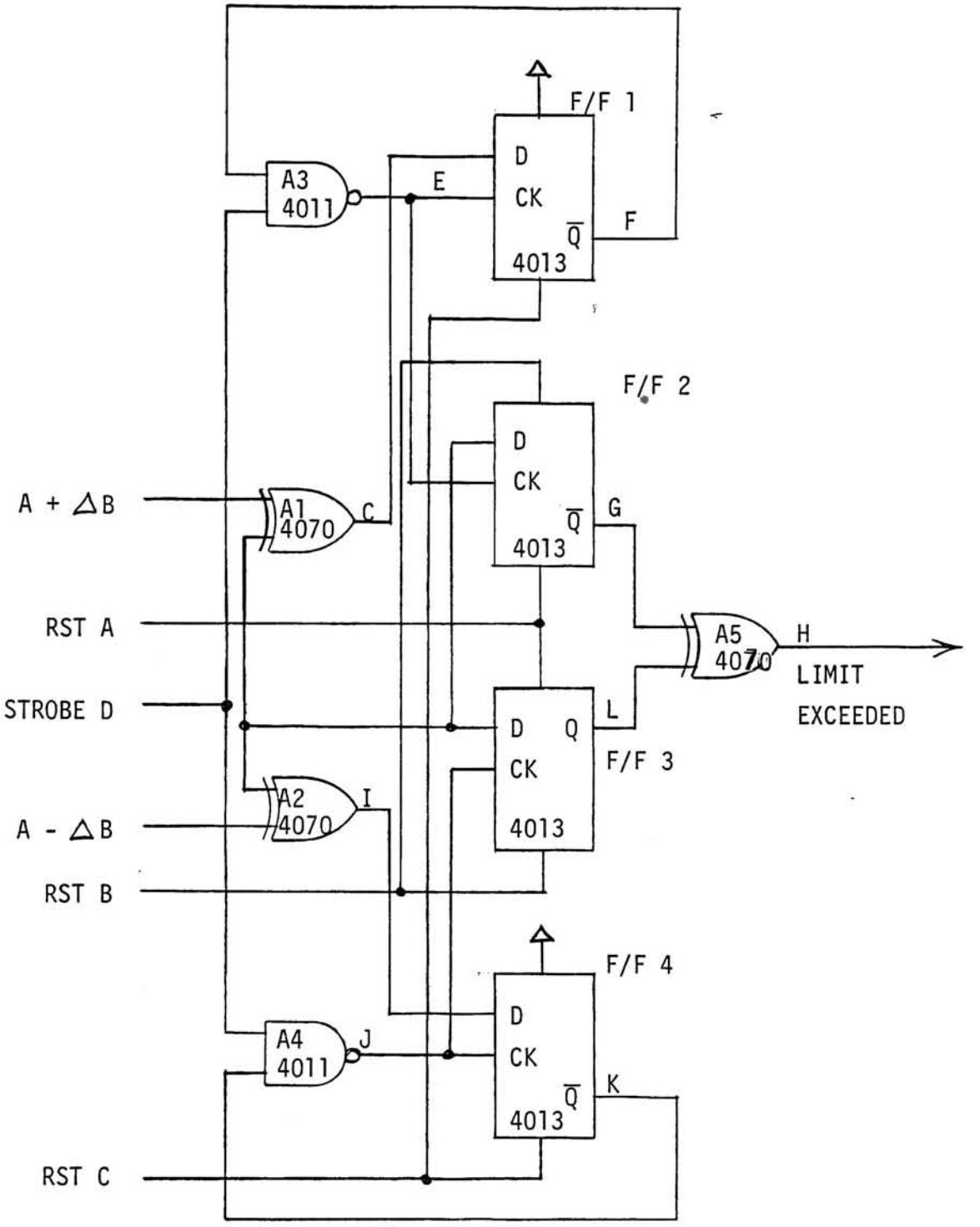


FIGURE 5.10 LOGIC DESIGN FOR UPPER/LOWER LIMIT DETECTION

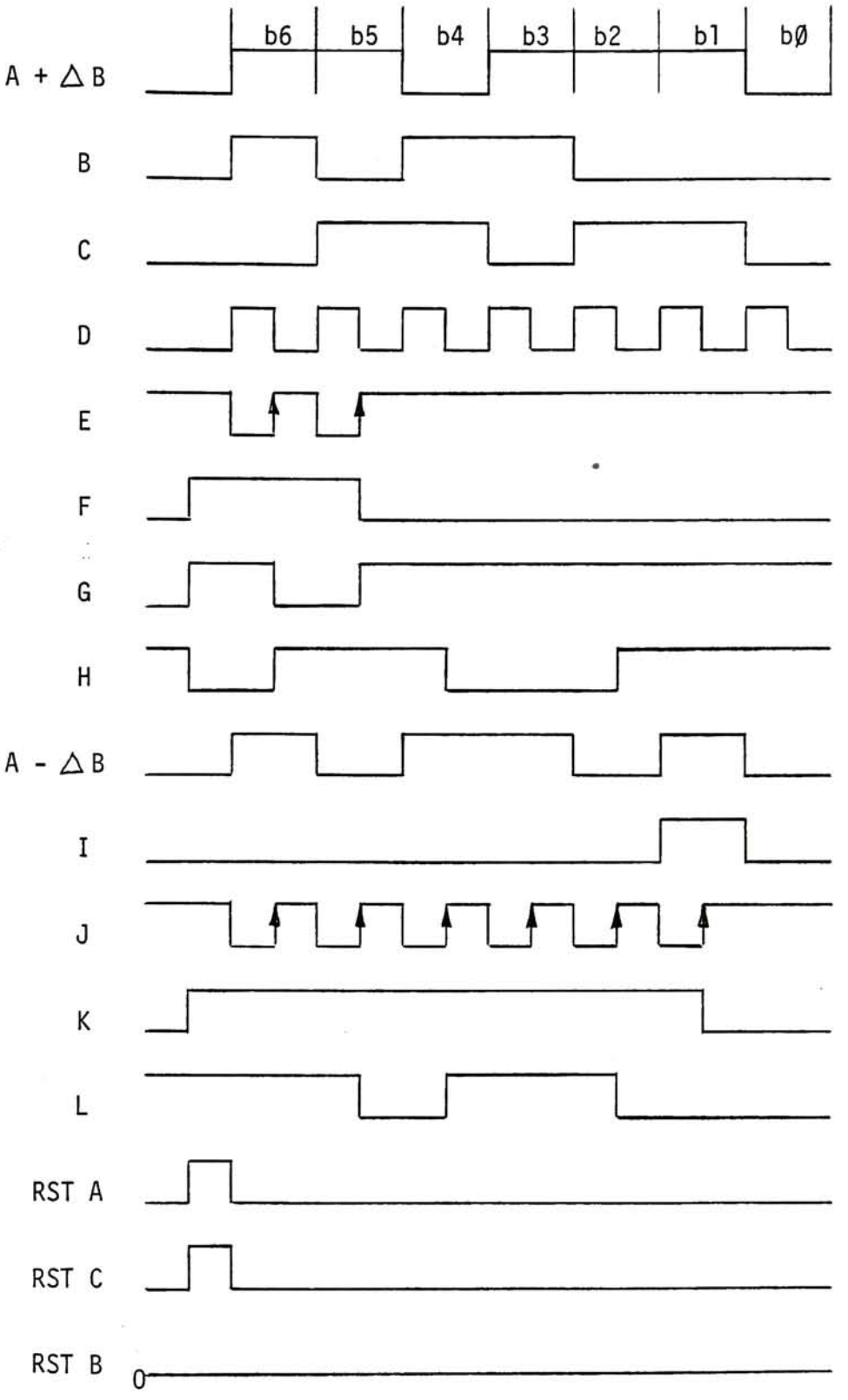


FIGURE 5.11 TIMING FOR UPPER/LOWER LIMIT DETECTION LOGIC.

a logic Ø. Signal F inhibits further strobe pulses at point E for the remaining bits. Since bit b5 of B is a logic Ø, F/F-2 remains in the reset state for the remainder of the compare test.

When A $-\Delta B \neq B$ during bit b1 then signal I goes true, causing F/F-4 to become set on the trailing edge to signal J. Signal K then inhibits further strobe pulses from passing thru gate A4 to point J. Since B was a logic Ø for bit b1, F/F-3 remains in the reset state for the remainder of the compare test and point H terminates in the logic 1 state.

As long as both C and I go true at least once during a compare test, then the final state of point H is independent of initialization with RST A or RST B. If B is equal to A $+\Delta B$ or A $-\Delta B$ then the final state of H is dependent on which reset is used to initialize F/F-2 and F/F-3.

Applying the data values shown in Table 5.1-(d) to the circuit of Fig. 5.10 results in no strobes existing at E and a final logic 1 strobed into F/F-3. If RST A was used for initialization, G would remain at a logic 1, causing H to terminate in the logic Ø state. If RST B was used for initialization, G would remain at a logic Ø, causing H to terminate in the logic 1 state. When the same conditions are applied for application of the data values shown in Table 5.1-(e) the termination of signal H is a logic Ø when RST A is used and a logic 1 when RST B is used.

Table 5.2 shows the final state of H for conditions (a) thru (e) of Table 5.1. Note that when RST A is used for initialization that the final state of H is low (logic Ø) when data B

TABLE 5.2

FINAL STATES OF SIGNAL H

DATA INPUT CONDITIONS	INITIALIZE WITH RST A	INITIALIZE WITH RST B	FINAL STATE OF OUTPUT H
SEE FIG. 5.9 - (a)	X	X	Ø
SEE FIG. 5.9 - (b)	X	X	1
SEE FIG. 5.9 - (c)	X	X	1
SEE FIG. 5.9 - (d)	1	Ø	Ø
SEE FIG. 5.9 - (d)	Ø	1	1
SEE FIG. 5.9 - (e)	1	Ø	Ø
SEE FIG. 5.9 - (e)	Ø	1	1

NOTE:

1 = TRUE = HIGH LEVEL

Ø = FALSE = LOW LEVEL

X = IRRELEVANT

is equal to the upper or lower limit. When RST B is used for the same conditions the final state of H is high (logic 1). This enables the system to detect an out-of-limit condition when data (A) is equal to the allowable deviation (ΔB) or when it is greater than the allowable deviation by one count.

One other condition exists which can cause a problem if RST B is used. This condition is when $\Delta B = \emptyset$. This can occur when the data value falls to 49 or lower and the percent deviation is 1 percent. When this condition exists and RST B is used, each conversion of the value 49 will cause ΔB to equal zero and H to be true. If RST A is used instead, then continuous conversions of 49 will cause H to be false. A problem occurs when the voltage value into the A/D converter is at a boarder point, causing the conversion value to alternate between 49 and 48, or any other two values below 50. Even the use of RST A causes every 1-count fluctuation of the digital conversion to produce a true H termination because ΔB equals zero.

This problem can be resolved by modifying the logic which produces the value of ΔB. The modification shown in Fig. 5.12 will assure that the minimum value of ΔB is one.

Point A1 (Fig. 5.12) was previously tied to point A3. Point A1 is the LSB of the binary value of ΔB which is stored in the binary counters (types 74LS197 and 4024). When point A1 is disconnected from point A3 and tied to the modified circuit (shown in dashed lines), then the multiplexed value of ΔB will always be one or greater.

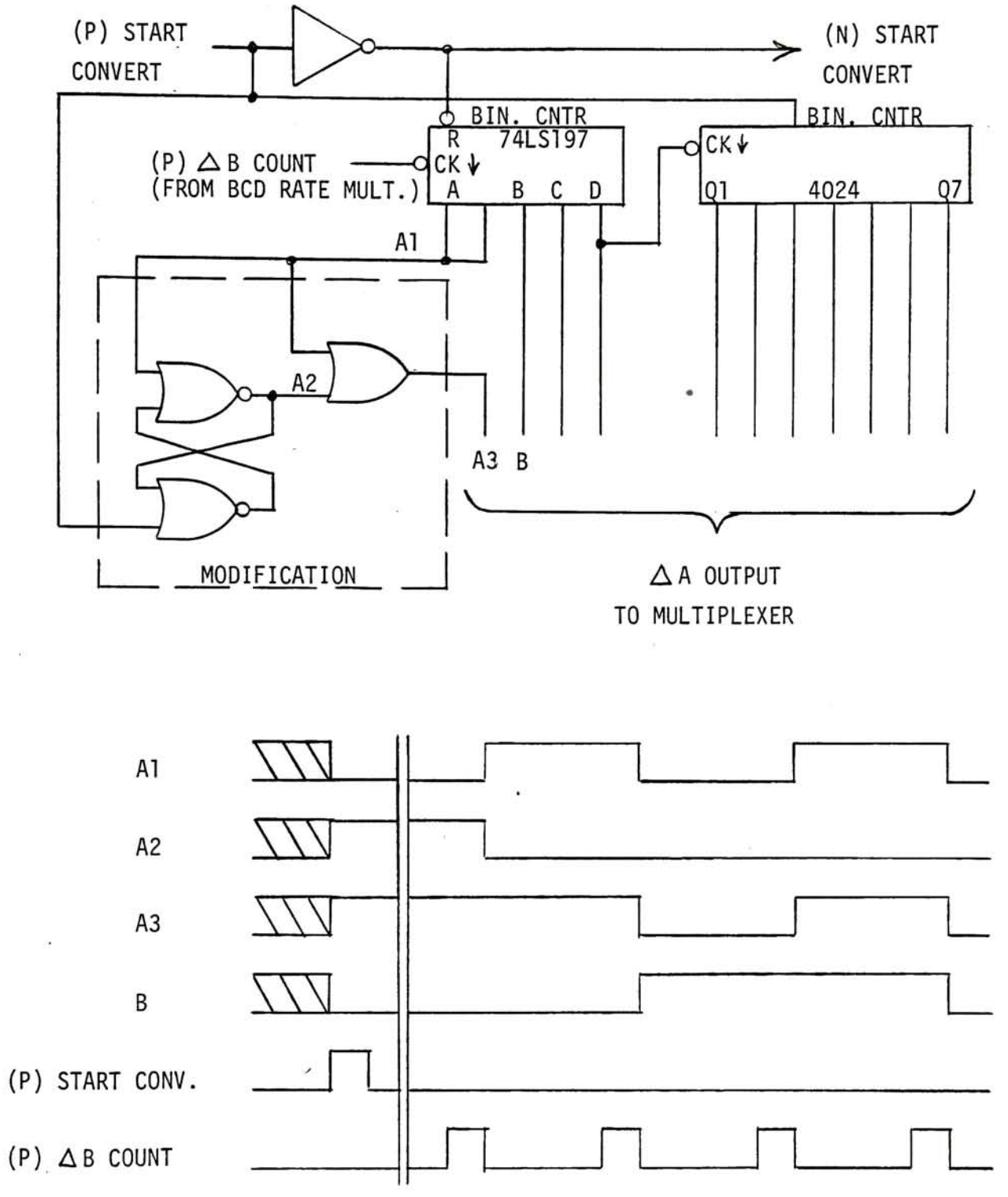


FIGURE 5.12 MODIFICATION OF △A COUNTER TO OBTAIN A MINIMUM VALUE OF ONE.

The timing diagram shown in Fig. 5.12 illustrates the relationship of the stored ΔB and the modified LSB (A3) of ΔB. Note that the "ΔB" counter is actually the "ΔA" counter (by definition) because the stored value of A and ΔA is designated as B and ΔB respectively. It is more convenient to refer to ΔB because this is the value used in equations 5.1 and 5.2.

Equation 5.2 is modified by a definition of ΔB:

$$\Delta B \geqslant 1 \qquad \text{(Eq. 5.3)}$$

One additional feature would involve inhibiting data compare when A is near zero. There are a number of transducers and transducer applications where the analog value is unstable near zero volts. This condition would cause the compare detection to continuously detect an out-of-limit condition with resultant printout. This undesirable condition can be eliminated by inhibiting the compare function when A is between 0 and, say, 15 counts. This data range then causes an inhibit of data compare for the lower .75 percent of a full scale range of 1999.

The circuit shown in Figure 5.13 performs the function of compare inhibit when $A \prec 16$. This value can be increased, if desired, by simply detecting successive connections from the 4024 binary counter to the 8-input NOR gate (type 4078). The "(P) INH - Ø" signal remains high when the data value is less than 16 causing flip-flops F/F 2 and F/F 3 (Fig. 5.10) to stay reset and set respectively and causing output H to terminate in the low state.

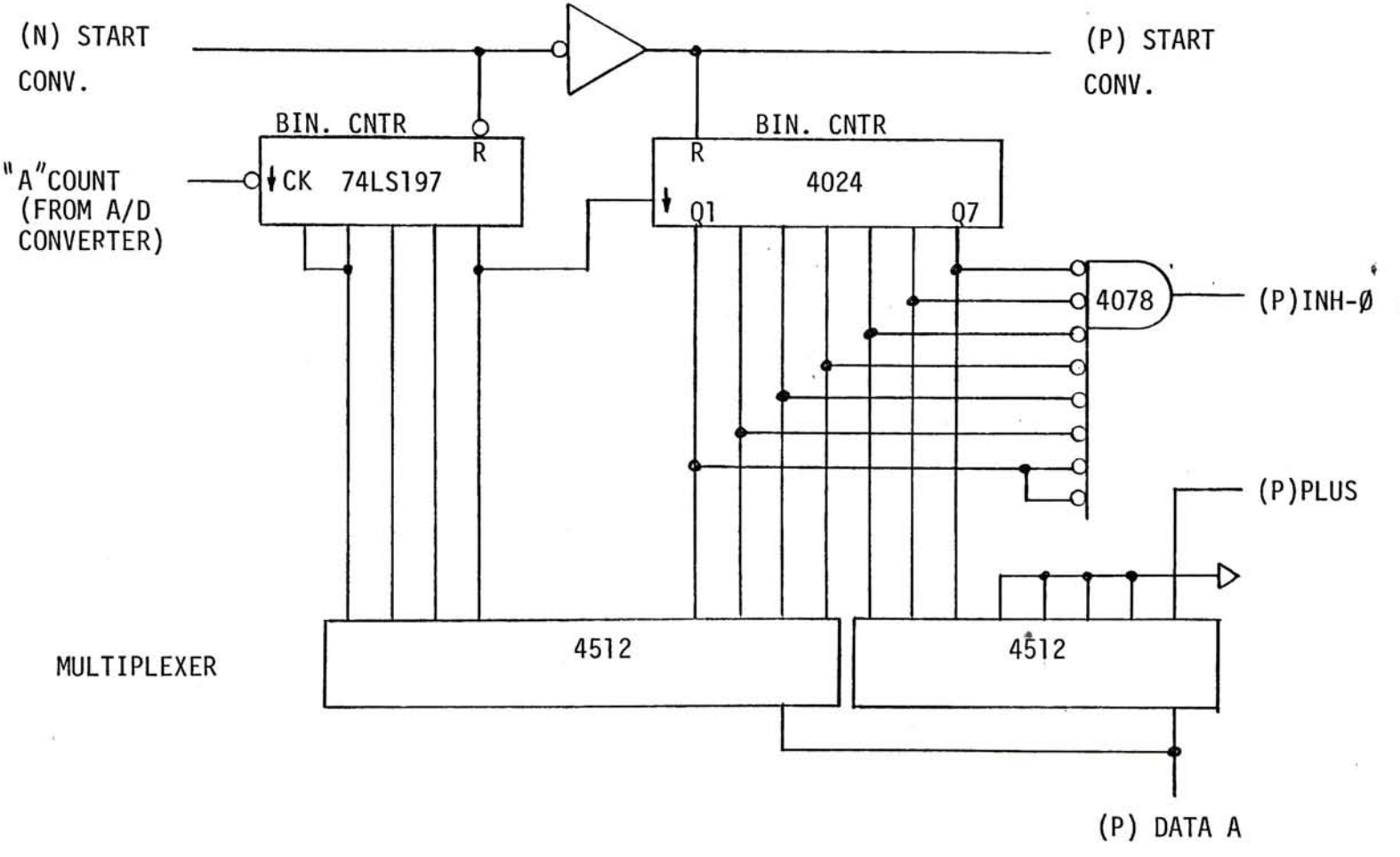


FIGURE 5-13 BINARY COUNTER FOR DATA VALUE A WITH "INH-Ø" ADDITION.

5.3.4 Data Compression Timing

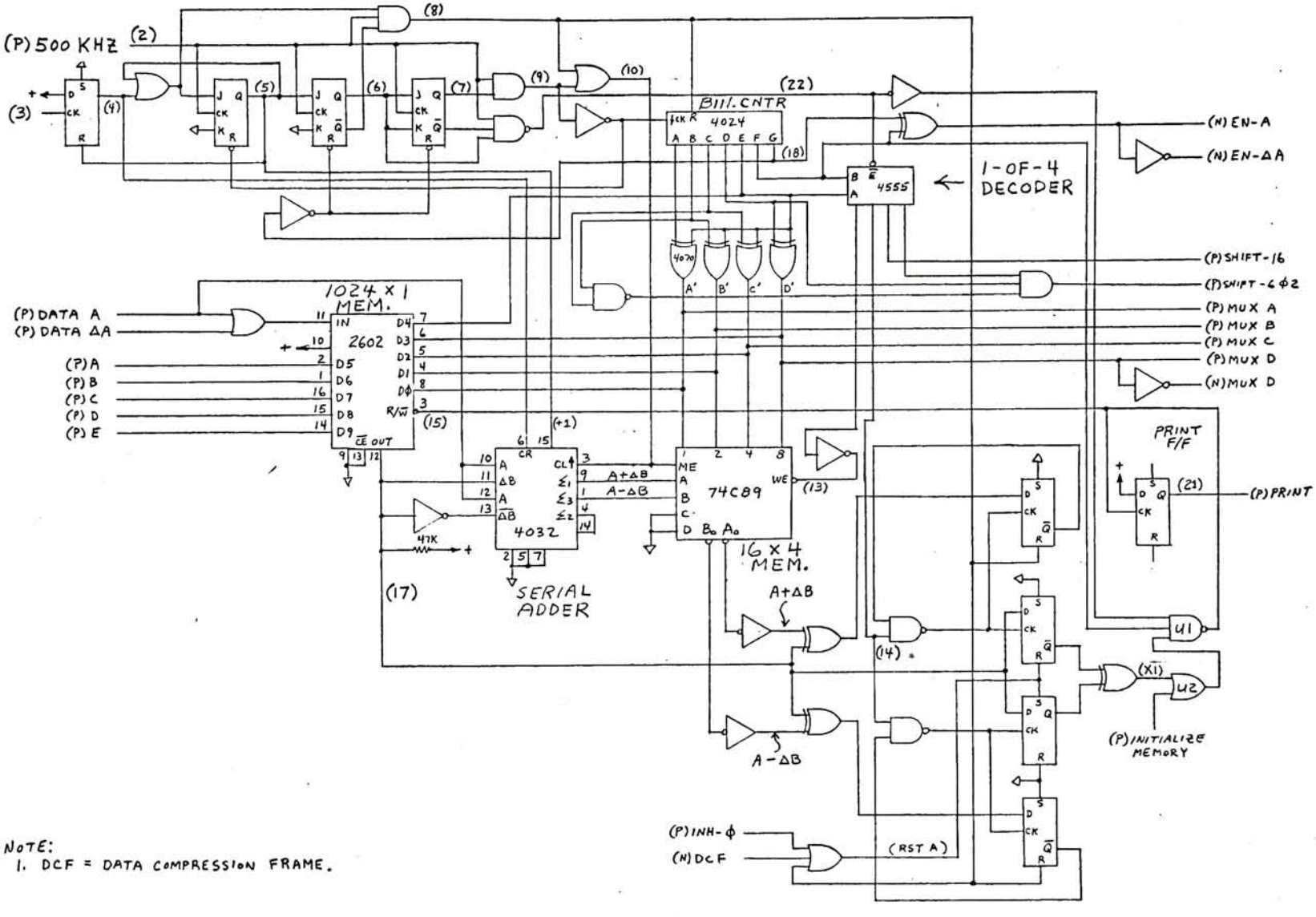
Figure 5.15 shows all the timing requirements of the limit compare logic. The waveforms are numbered on the right hand border for easy reference. The same waveform numbers are shown in Figure 5.14 at the point where the waveform originates.

In STEP 1 the upper limit (A $+\Delta B$) and lower limit (A $-\Delta B$) is calculated simultaneously. This is accomplished with the CMOS type 4032 triple serial adder shown in Figure 5.14. Waveform No. 16 and 19 shows the sequence in which ΔB and A are read respectively.

The serial bit summation is stored in temporary RAM (74C89) as shown in Figure 5.14. The write pulses are shown in waveform No. 13 of Figure 5.15 with the corresponding 74C89 memory addressing as shown in waveform No. 12. Note that the input address, waveform No. 11-b, is latched into the 74C89 on the positive-to-negative transition of waveform No. 10.

The comparison of new data with the upper and lower limits is also accomplished on a bit-serial basis, but starts with the MSB and sequentially progresses to the LSB as shown in STEP 2 of Figure 5.15. Note that the addressing sequence shown in waveform 12 starts with address 15. Limit detection is performed with the compare pulses shown in Figure 5.15-(14). If data A has exceeded its limits then the PRINT flip-flop (Fig. 5.14) will become set at the time shown in Figure 5.15 - (21).

The PRINT flip-flop is initialized (reset) at the beginning of each data frame. If the PRINT flip-flop is set during a data compression frame, then an ASCII "CR" code is trans-



NOTE:
1. DCF = DATA COMPRESSION FRAME.

FIG. 5.14 LIMIT COMPARE LOGIC

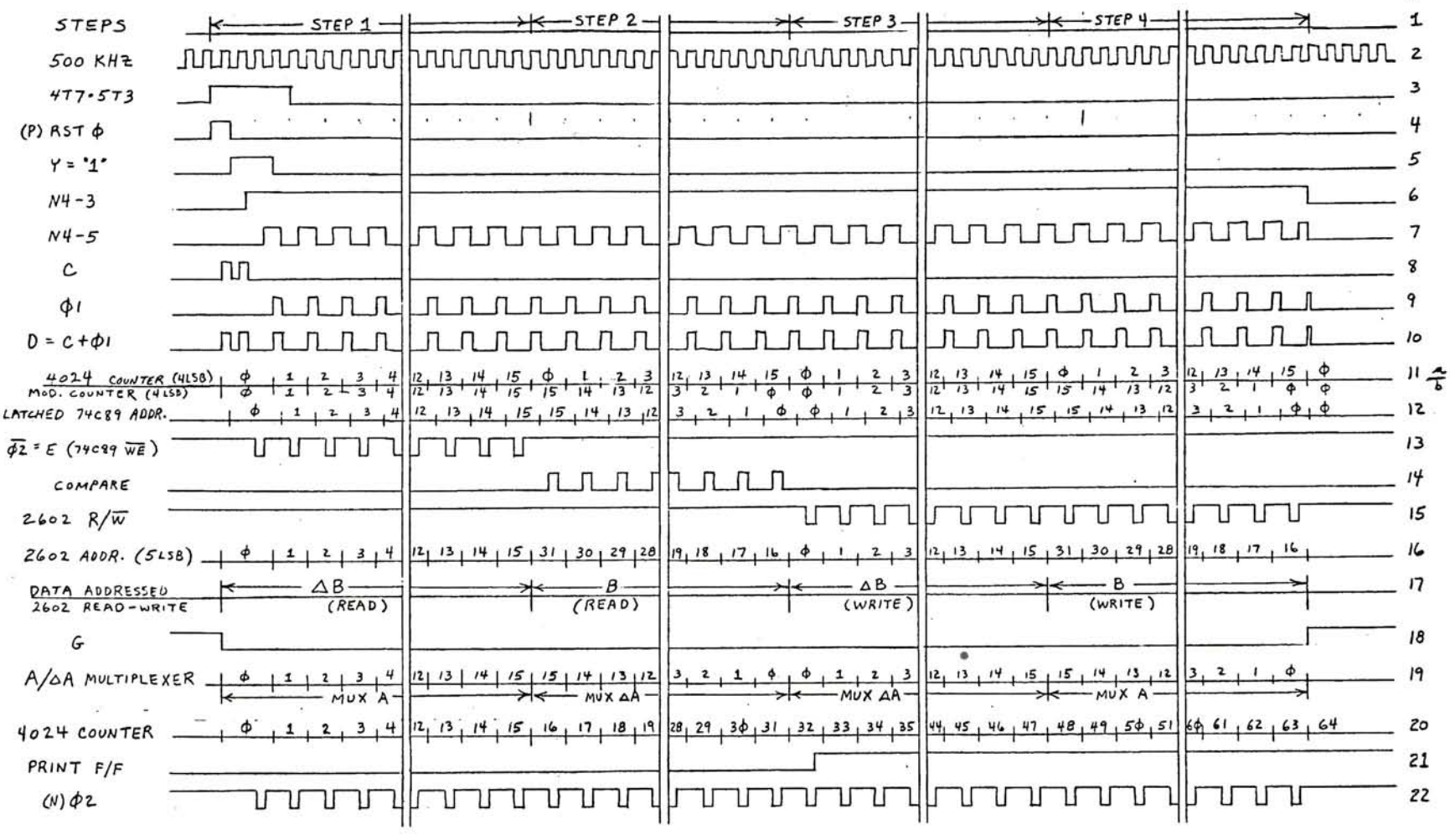


FIG. 5.15 LIMIT COMPARE TIMING

mitted to the line printer buffer during channel 21 multiplex time, causing the line printer to print the data buffer contents. The print mode is discussed in detail in paragraph 5.5.

Each time a data value exceeds its limits the exclusive - OR gate output (Fig. 5.14) at point 1 goes true. This condition partially enables the 3-input NAND gate (U1). When output F of the 4024 counter also goes true then 16 pulses at point (22) are gated thru gate U1 to point (15) [see Fig. 5.15 - (15)]. The write pulses at this point cause ΔB and B to be updated in the 2602 RAM during STEPS 3 and 4. Note the bit-write sequence in Fig. 5.15 - 16 and 17. The actual data written into the 2602 RAM is ΔA and A as shown in Fig. 5.15 - 19, STEPS 3 and 4. First, ΔA is multiplexed and stored in STEP 3. The storage sequence begins with the LSB as shown in Figure 5.15 - 16, STEP 3. Next, A is multiplexed and stored in STEP 4. The storage sequence begins with the MSB as shown in Figure 5.15 - 16, STEP 4.

All the analog data (A and ΔA) is written into the 2602 RAM for the first data frame following the activation of the "PRINTER ON" switch. This initialization of memory is accomplished by making the "(P) INITIALIZE MEMORY" signal true during the first data frame. This causes the PRINT flip-flop to become set during the first analog data channel, with subsequent printout. The sequencing of data bits as shown in Fig. 5.15, STEPS 1 thru 4 is easily accomplished by using a CMOS 4024 binary counter followed by four EXCLUSIVE - OR gates (Type 4070) as shown in Figure 5.14. Output E of the 4024 counter is used to invert (reverse) the count sequence of outputs A thru D at points A' thru D' during STEPS 2 and 4 via the four EXCLUSIVE - OR gates. The real

count of the 4024 and the modified count (MOD, COUNT) are shwon in Fig. 5.15 - a and b respectively (for the 4 LSB's). The 5 LSB's of the 2602 RAM are shown in waveform 16 and the full (real) 4024 count sequence is shown in Fig. 5.15 - (22).

At count 64 the G-output of the 4024 counter goes true, resetting flip-flops U3 and U4 and terminating the timing sequence for the data channel. Since a clock frequency of 500 KHZ is used, total elapsed time for STEPS 1 thru 4 is 259 microseconds. Also, since STEP 1 started 730 microseconds into the 1,000 microsecond data channel select time, then STEP 4 is completed 11 microseconds before the end of the data channel select time!

The final schematic for the Data Compression sub-system is shown in Figure 5.16. The logic which is located in the lower left corner is required for data compression control. The five outputs which terminate in rectangular-shaped pins are used for multiplexing the digital data channels to the main logic.

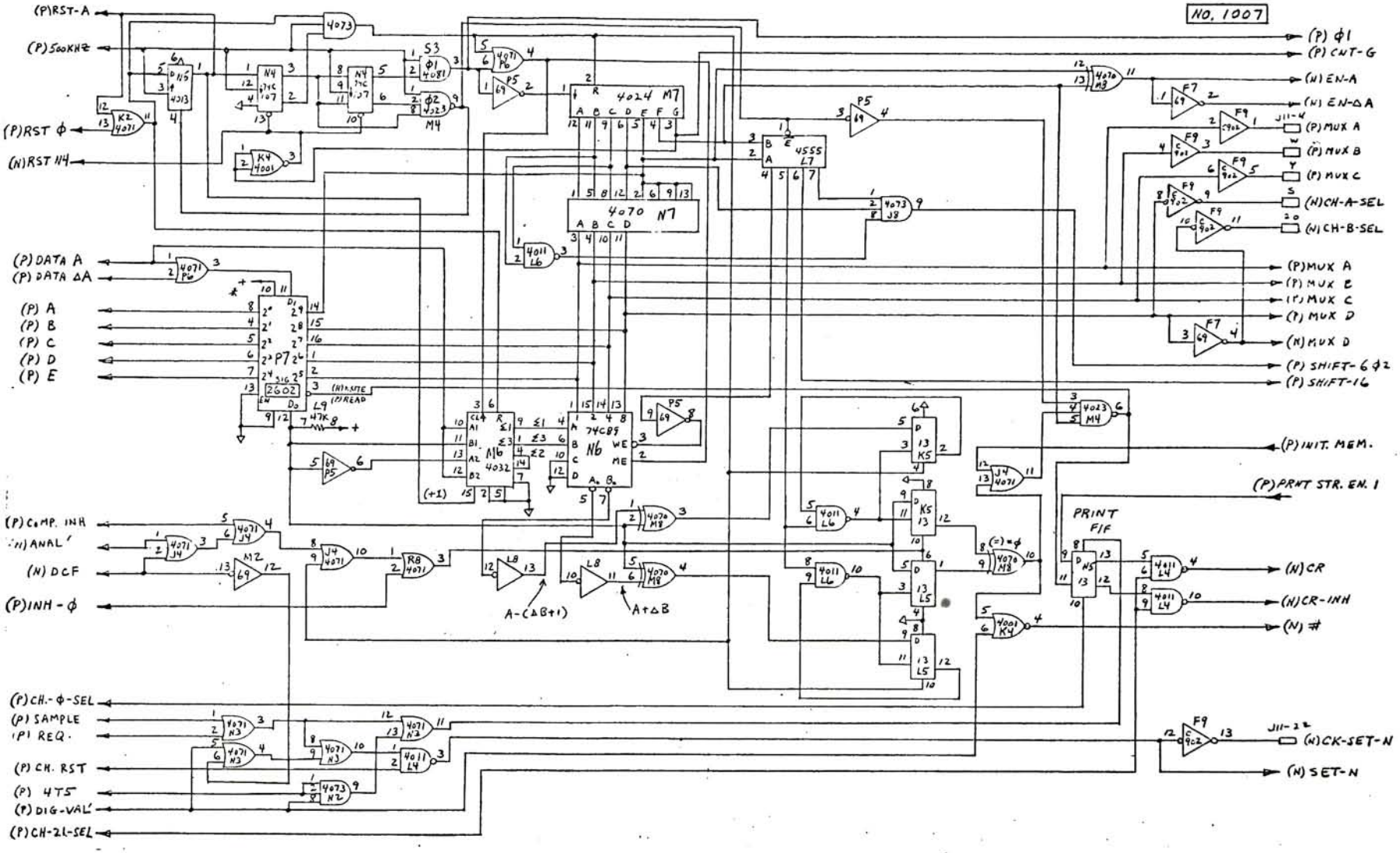


FIGURE 5.16 FINAL DATA COMPRESSION SUB-SYSTEM

5.4 The A/D Conversion Sub-System

A functional block diagram of the A/D conversion sub-system is shown in Figure 5.17. The primary components of this sub-system are the analog multiplexer, absolute value circuit, A/D converter, and digital multiplexer (MUX). The secondary components consist of the voltage references, binary data tolerance conversion, and binary data conversion. The design for each of these sub-system components is performed in paragraphs 5.4.1 thru 5.4.7.

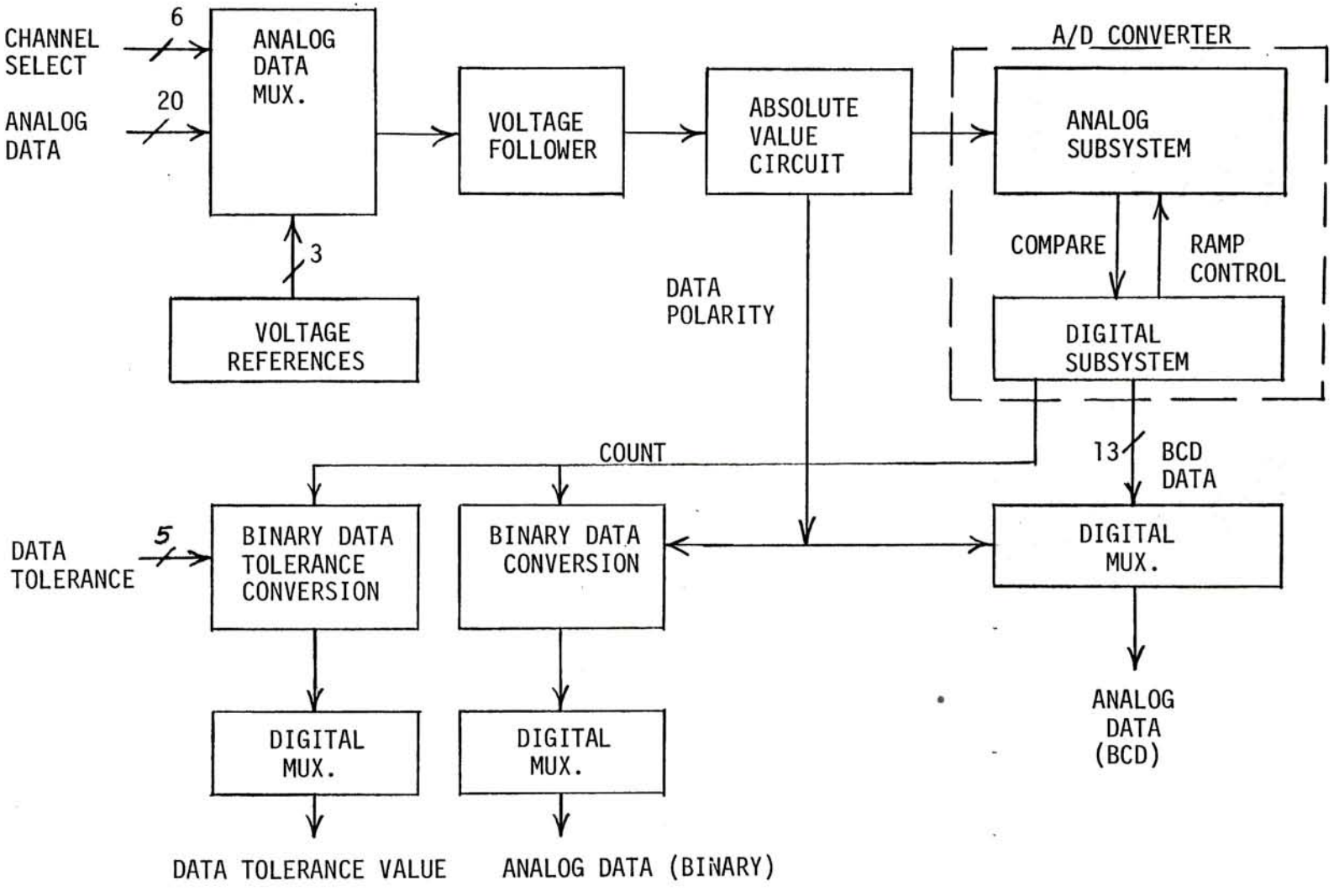


FIGURE 5.17 BLOCK DIAGRAM OF A/D CONVERSION SUBSYSTEM.

5.4.1 The Analog Multiplexer and Voltage Follower

The analog data multiplexer multiplexes 20 bipolar analog channels and 3 voltage references as shown in Figure 5.17. The voltage follower is required to eliminate analog errors due to analog channel output resistance and multiplexer ON resistance variations. These variations can produce a (unity) gain error in absolute value circuit.

The analog multiplexing circuit is shown in Figure 5.18. The AM3705[8] is an 8 channel MOS analog multiplexer made by National. Three multiplexers are required for the 20 analog channels and three voltage references of 0.0V, -1.000V, and +2.000V. The actual voltages are -.9995V and +1.9995V. The AM3705 was selected because it is a 16 pin device and has a low cost.

The ON resistance of the AM3705 can vary from below 80 ohms to 400 ohms. This variation is eliminated by using a voltage follower as shown in Figure 5.18. The 10K ohm potentiometer is required to balance the input offset voltage. The 1 megohm resistor is required when an analog channel is selected, but does not exist. This condition presents an open circuit or floating input to the voltage follower, but the resistor causes zero volts to be applied to the input. The 510 pf capacitor is obviously used for filtering noise.

Inputs A thru G (lower left) are from the 7 stage binary counter which counts from Ø to 99 at a 1 millisecond rate. Input A is the LSB. The 4556 is a 1-of-5 decoder and is used here simply to select the three multiplexers in the proper sequence.

(8) National Semiconductor Corp., Linear Integrated Circuits, Jan. 1974, p. 7-24.

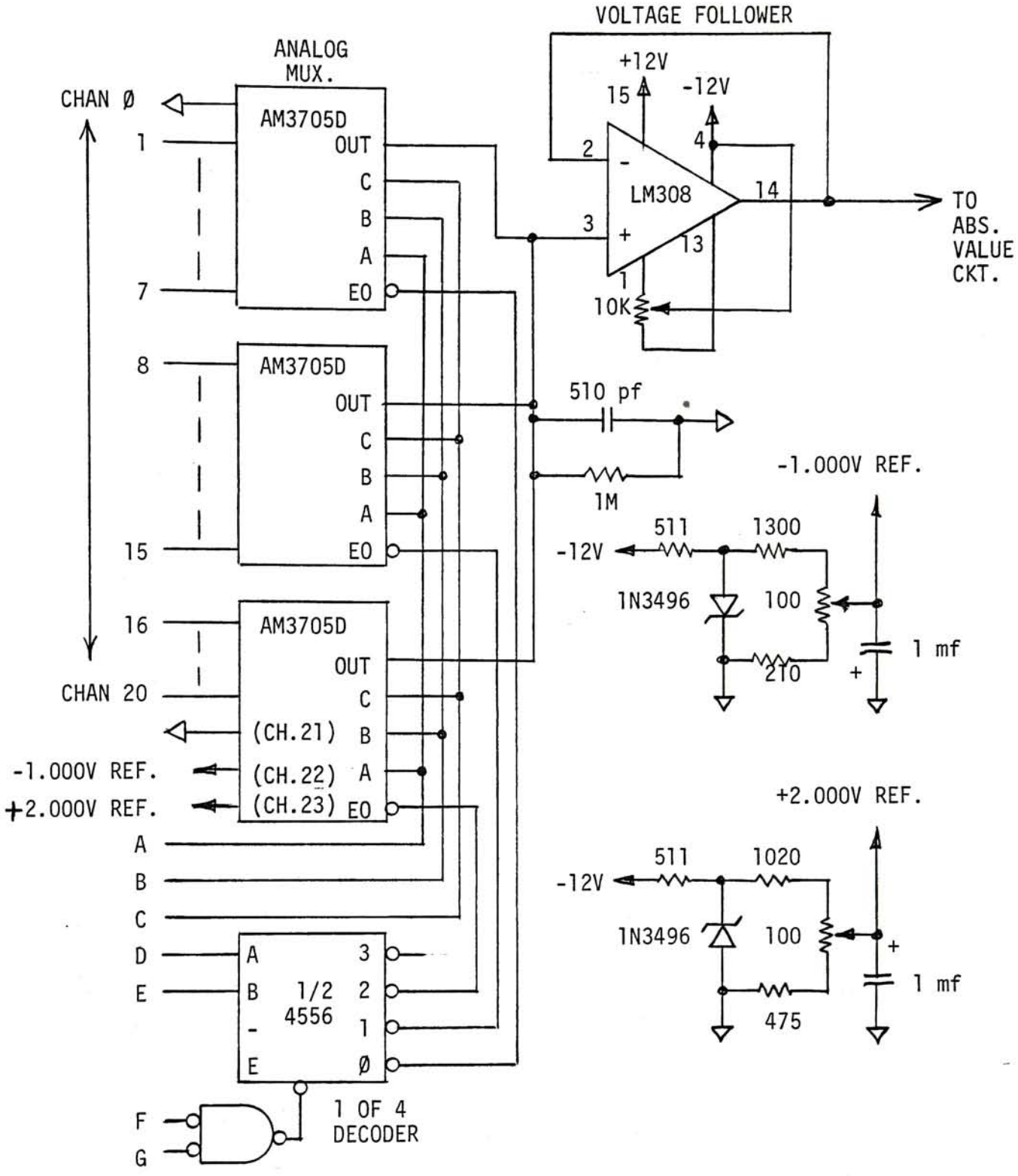


FIGURE 5.18 ANALOG MUX AND VOLTAGE FOLLOWER

5.4.2 The Absolute Value Circuit

The absolute value circuit shown in Figure 5.19 was acquired from Teledyne Philbrick's Application Bulletin AN-6, dated January 1974. The two 10K ohm offset potentiometers were not shown in the application bulletin, but were added to obtain better performance (accuracy) near zero volts. A 0.1 microfarad capacitor was also added to the base of the transistor to eliminate oscillations which may occur if the Input signal is near zero volts. The .01 microfarad capacitor is added to the output to reduce noise.

5.4.3 The A/D Converter

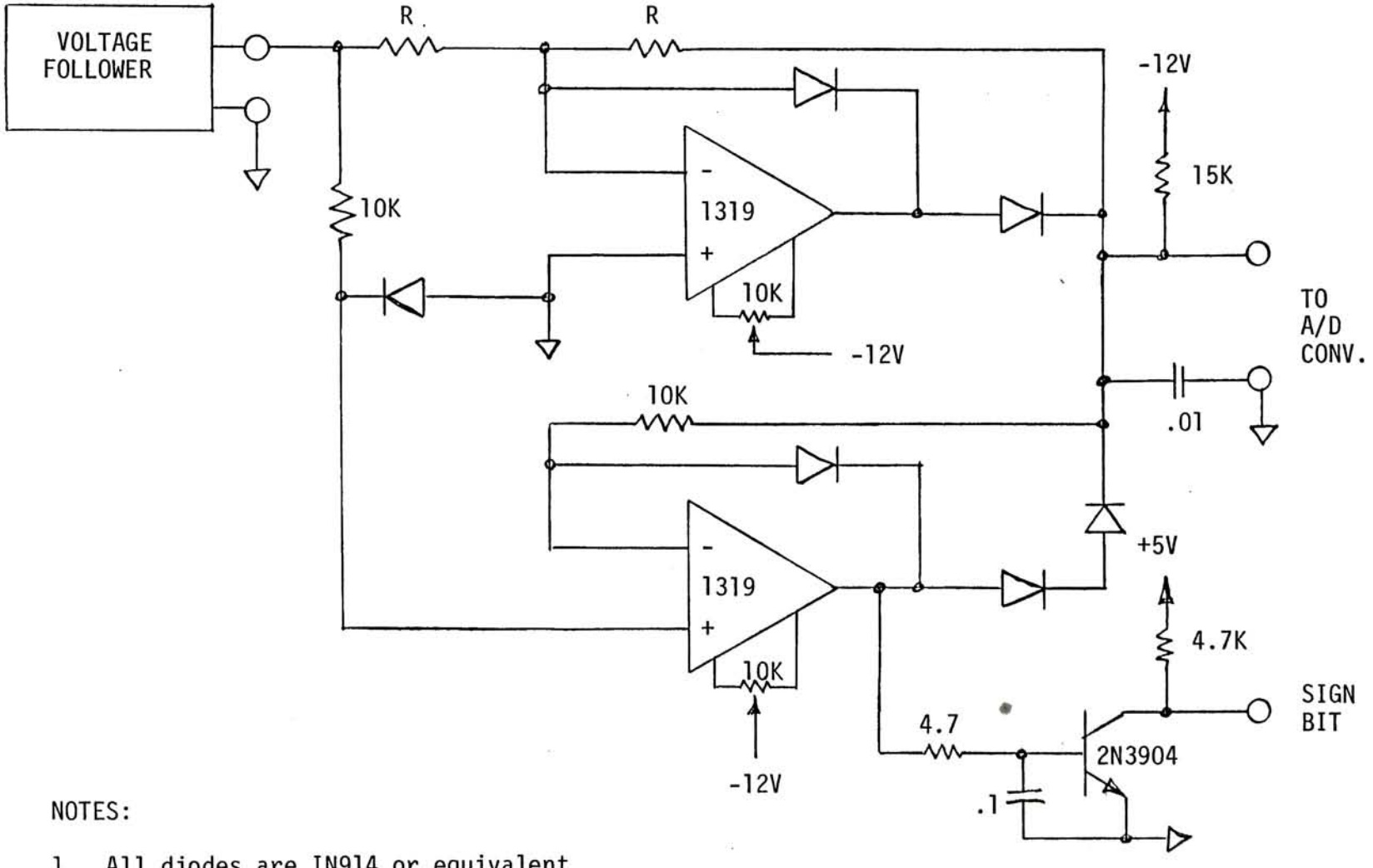
It was determined in paragraph 3.2.1, page 21 that a dual slope A/D converter will be used. A dual slope A/D converter consists of an analog and a digital sub-system as shown in Figure 5.17.

Motorola has an impressive 2-IC dual slope A/D converter using the MC1505[5] analog sub-system and the MC14435[5] digital sub-system. An attractive feature is that both IC's have 16 pins, requires a total of 8.8 ma at 5 VDC, and requires only one voltage. The MC14435 cannot be used because of its upper operation limit of 1 MHZ. This limitation exists because the MC14435 is CMOS.

The MC14435 digital sub-system can be designed using discrete CMOS digital IC's. The 74LS00 series can be used where high frequencies prohibit the use of CMOS logic.

Figure 5.20 shows the complete A/D converter sub-system which includes the analog multiplexer, reference voltages, voltage follower, analog/digital converter sections, the binary

(5) See Appendix A



NOTES:

1. All diodes are IN914 or equivalent.
2. All capacitance values are in microfarads.
3. R = 10K ohm, wirewound, $\pm$ .01%.

Figure 5.19 ABSOLUTE VALUE CIRCUIT

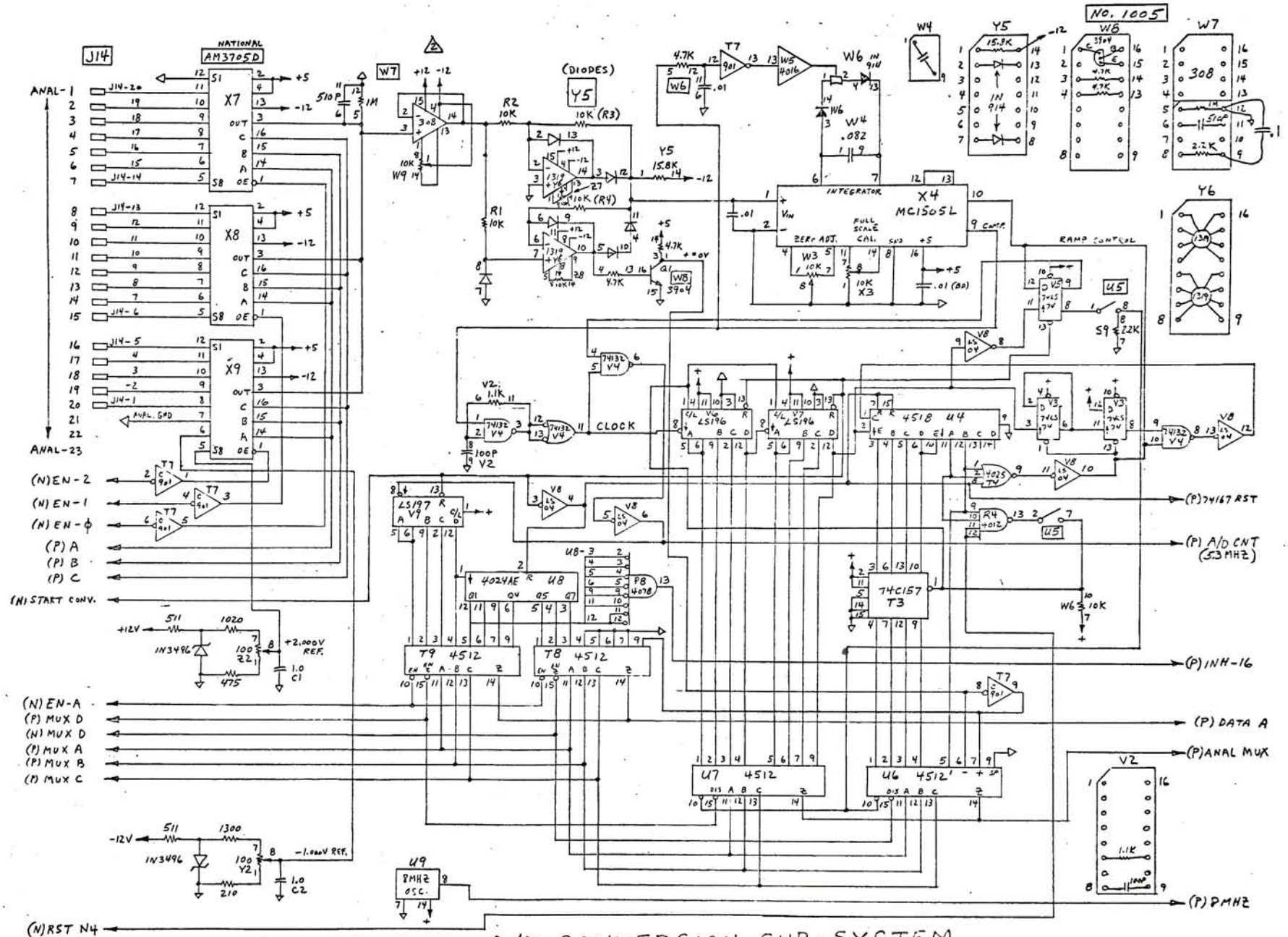


FIGURE 5.20 A/D CONVERSION SUB-SYSTEM

counter which obtains the binary data value, and the multiplexers for the BCD and binary data values. Each function will be described in detail.

The operation of the dual slope A/D converter sub-system[9] is fully described by Motorola and will be repeated here. The dual slope method of A/D conversion is a proven system which is capable of high accuracy. The conversion is an integrating process which offers high noise rejection and immunity to changes in the clock rate and integrator capacitor value. The particular method used in the MC1505 is a non-iterating dual slope technique which produces an accurate result after one conversion period.

Dual slope conversion is accomplished with the system of Figure 5.21. The conversion begins at time t1, when current I_X causes the integrator output, or ramp, to cross the comparitor threshold, as shown in Figure 5.22. The clock is activated and the counters begin counting from zero. The system counts for a fixed period T, with a ramp slope which depends on the input voltage, i.e., a steep slope is caused by a high input voltage. When the counters have reached full scale, the overflow counter triggers a ÷ 2 flip-flop which changes the ramp control polarity current. I_R now controls the integrator and and down ramp begins at t_2. This ramp continues at a fixed slope for a time period which depends on the amplitude achieved by the up ramp. Thus, T2 is determined by the input voltage. When the ramp crosses the comparitor threshold at t_3, the clock stops and the counter holds a digital value which is proportional to the unknown input voltage.

(9) Motorola Technical Information Center, Semiconductor Data Library, Linear Integrated Circuits, Vol. 6/ series B, pp. 5-31 to 5-34.

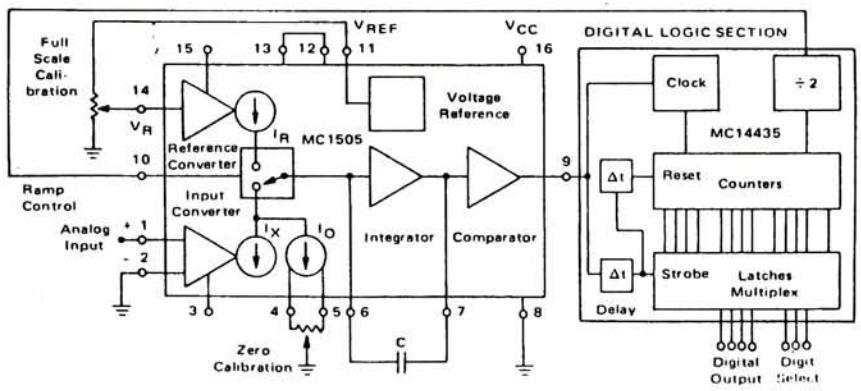


FIGURE 5.21 FUNCTIONAL DIAGRAM OF A/D CONVERSION

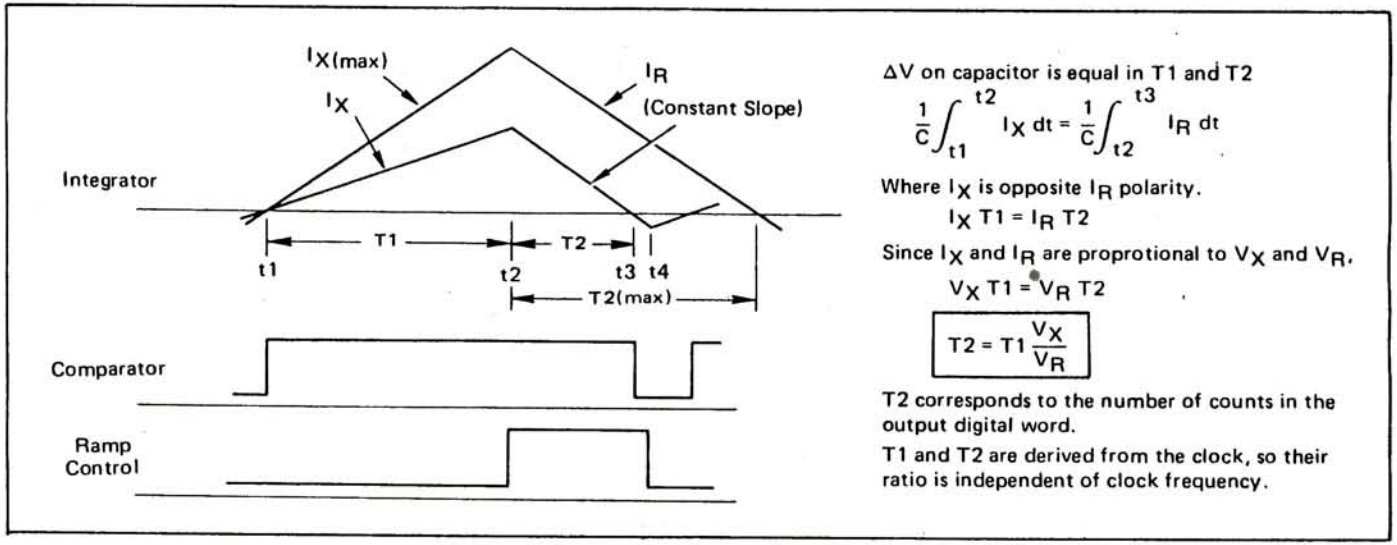


FIGURE 5.22 DUAL SLOPE A/D CONVERSION WAVEFORMS

Since the voltage change across the capacitor is equal on the up and down ramps, an equal amount of charge is exchanged. The equations of Figure 5.22 show that the system output is the ratio of the unknown and reference currents, and the long term changes in the clock rate and integrator capacitor do not effect the reading.

An important feature of the MC1505 is the ramp offset current source which is added to the unknown current and does not allow the ramp to reach zero slope when the input voltage is zero. The ramp range is shown in Figure 5.23. The ramp offset current has a value of $I_R/10$, so that the minimum ramp slope is 5 percent of the full scale slope. This allows reliable conversion at low input voltages by assuring a nearly constant comparator propogation delay and a good ramp signal-to-noise ratio. It also prevents turn-off of the diode in the current switch at low levels, restricting the voltage change at the output of the resistor bridge. Still another feature is that it provides a convenient temperature compensated zero adjust which can correct errors in the resistor bridge and input buffer amplifiers when they are used. The ramp offset current is compensated by 100 extra counts in the digital logic during ramp down, so it does not appear in the digital output (see Figure 5.23).

The operation of the A/D converter is Figure 5.20 will be described using the timing diagram in Figure 5.24. The "(N) START CONV." pulse resets all counters and flip-flop V5 when it is at zero volts. When this signal goes high the RAMP CONTROL (V8-10) goes low, causing the integrator to start charging and holding both flip-flops in location V3 reset. When the integrator charges up to +1.00 volts the COMPARE

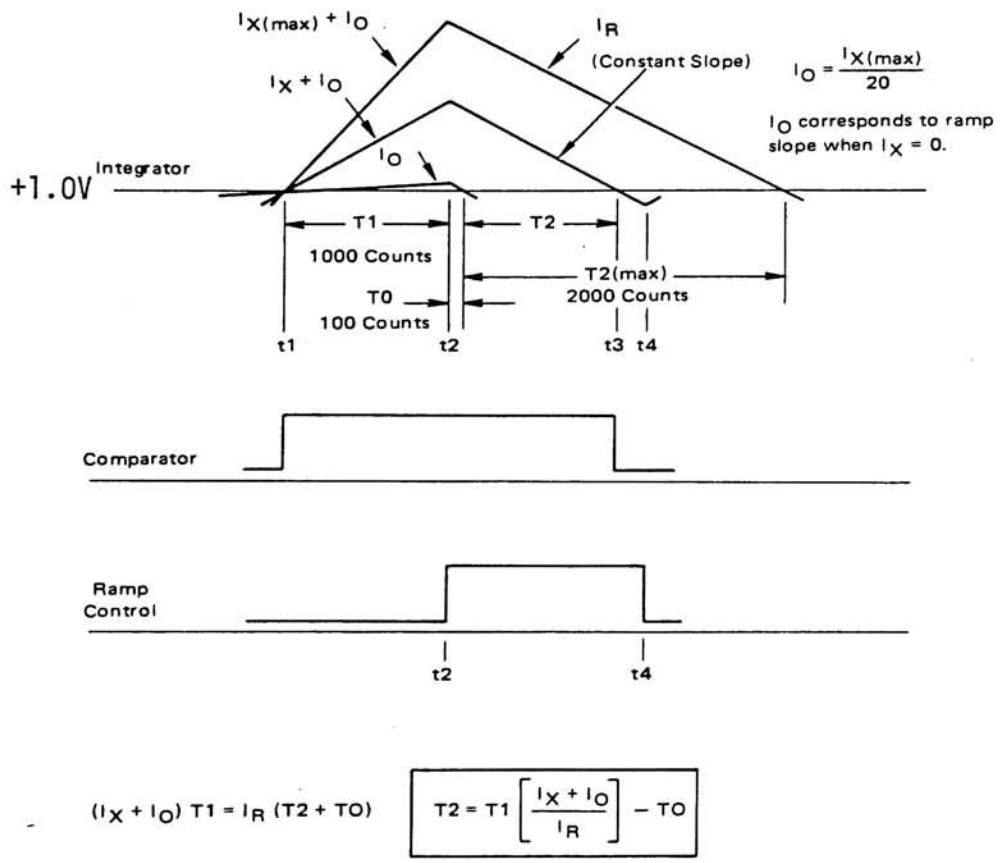


FIGURE 5.23 MC1505 SYSTEM TIMING DIAGRAM

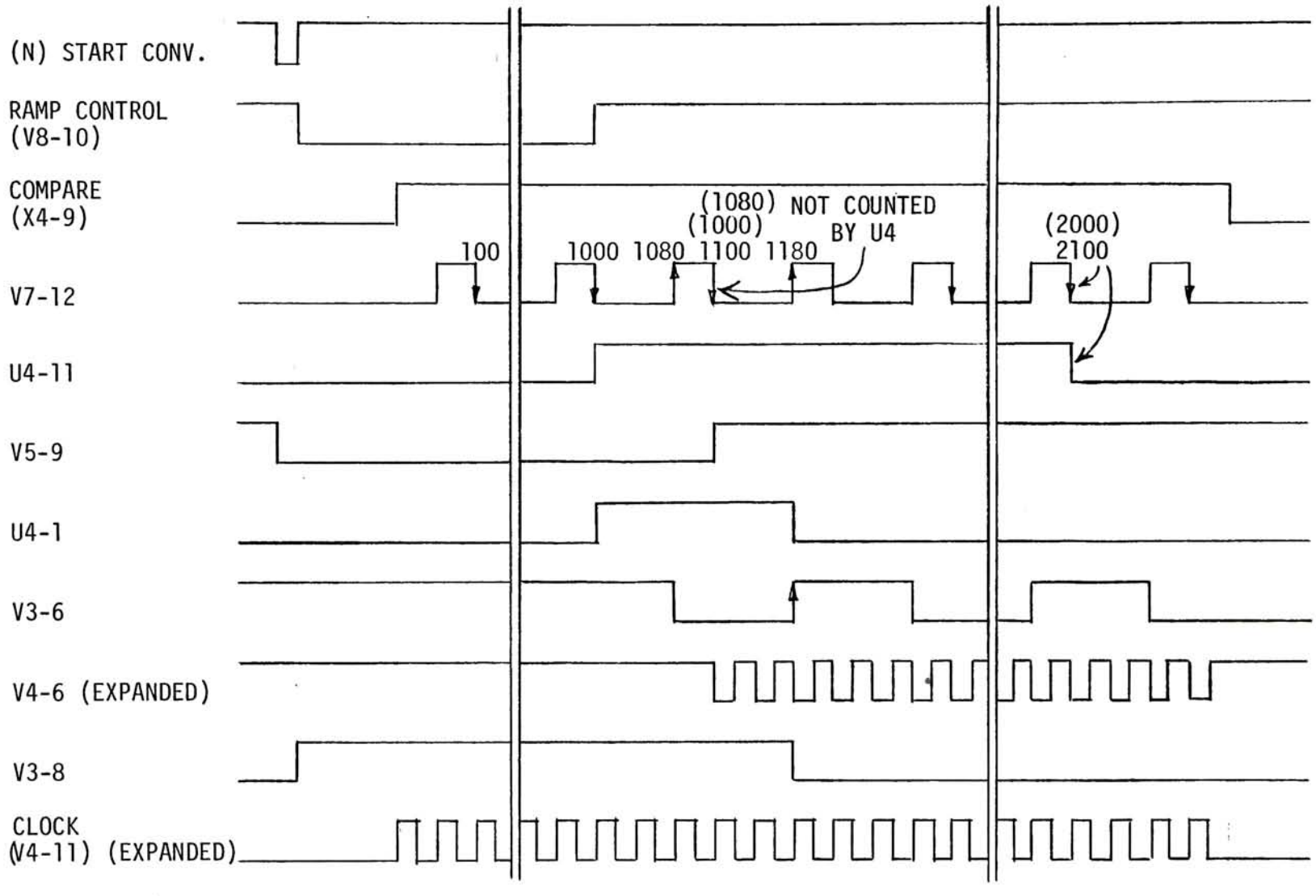


FIGURE 5.24 - DIGITAL SUBSYSTEM TIMING FOR A/D CONVERTER

signal from the MC1505 goes high, enabling the clock (V4-11). The clock operation is discussed in paragraph 5.4.4. Counters V6 and V7 must be selected from the 74LS00 series because the clock frequency is 5.33 MHZ, which is too fast for CMOS. Counter V7 must be fast because it must enable the clock frequency at V4-6 via V8-8 and V5-9, which must also have a fast response, so that a clock pulse is not missed at V4-6.

When count 1000 is reached, U4-11 goes high, causing the RAMP CONTROL signal to go high and taking the reset off of flip-flops V7- 1 and 13. The integrator now discharges. Note that U4-12 is used as the "1000" digit by the multiplexer instead of U4-11. The multiplexer therefore sees zero count when the counter is actually at count 1000. At count 1000 the signal at U4-1 goes high, causing counter U4 to become disabled.

At count 1100 flip-flop V5-9 becomes set, enabling the remaining clock pulses to pass thru gate V4-6. Since the remaining pulses from V4-6 are equal to the data value, they are used to obtain the binary value of the data in counter V9 and U8. The count pulses are also used to obtain the binary value of the product of the channel tolerance and channel data value. This product is referred to as ΔA, and the logic required for obtaining it is described in paragraph 5.4.7. Notice that the waveform for V7-12 in Figure 5.24 includes parenthesied numbers above all numbers that are 1100 and greater. These numbers are the actual counter contents because at count 1100 counter U4 did not increment, thereby losing a 100-count pulse and causing the counter to contain

count 1000. This loss of 100 counts compensates for the ramp offset current, as previously described. Also notice that the multiplexer sees a count of zero.

At count 1180 flip-flop V3-8 becomes set, causing the voltage level at U4-1 to go low, and again enabling counter U4. Notice that only one clock pulse was not counted by U4. Since each pulse represents 100 counts, then the requirement to obtain a count-offset of 100 counts has been satisfied. Also notice (see Figure 5.24) that gate V4-6 is enabled at count 1100, or 100 counts after the down ramp of the integrator began. This 100 count delay compensates for the ramp offset current as previously described.

If the count reaches ("2000"), U4-11 goes low and U4-12 goes high, maintaining a high level on the input of gate T4-9. U4-12 is also tied to the BCD multiplexer and represents the "1000" digit.

When the integrator voltage finally goes 0.1 millivolts below the comparator reference voltage of +1.00V the COMPARE signal goes low and inhibits the CLOCK. The BCD and binary counter multiplexers now contain the same data value. The proper ΔA value is also contained in the ΔA binary counter.

5.4.4 Increasing the A/D Converter Speed and Accuracy

The initial design of the A/D converter did not have the circuitry across the integrator capacitor as shown in Figure 5.20. This resulted in a 590 microsecond delay between the "(N) START CONVERT" pulse and initiation of the COMPARE signal for an A/D input of zero volts. A COMPARE time of 135 microseconds (clock = 5.3 MHz) resulted in a total conversion

time of 725 microseconds. Only 644 microseconds are available for A/D conversion during a 1.0 millisecond channel-select time. The remaining 356 microseconds are required for analog multiplex and settling time (see para. 4.1.2.(a), page 85). and the data compression timing (see para. 4.1.2.(c), page 85).

The 590 microsecond delay is required because the compare voltage at point A of Figure 5.25 decreases to approximately 0.1 volt between conversions. When zero volts is converted, the resulting small integrator capacitor current, I_0, results in a 590 microsecond charge time for the voltage at point A to reach the comparator reference of 1.0 volt.

When two silicon diodes are placed in parallel with the integrator capacitor (Fig. 5.25) they serve as a voltage clamp, allowing the voltage at point A to go no lower than 1.30 volts below the voltage at point B. Since the voltage at point B is always +1.95 volts, point A is not able to go lower than: 1.95 - 1.30 = +.65 volts. Now when a conversion is initiated, point A must only charge +.35 volts to reach the 1.0 volt compare reference. Since the charge slope of I_0C has not changed, the time, t_f, to reach the compare voltage is: $t_f = (.35)(590)/.9 = 220 \times 10^{-6}$ sec.

The diodes solved the compare delay problem, but caused the integrator slope to become non-linear because current passed thru them until point A charged up to approximately +1.1 volts. The same problem existed during the down slope in the range of +1.1 volts to +1.0 volts. This problem was resolved by adding an analog switch in series with the diodes as shown in Figure 5.20, and controlling the ON/OFF time with the COMPARE signal. When the integrator voltage at point A is above 1.0 volts, the COMPARE signal goes true and the diode path becomes open circuited.

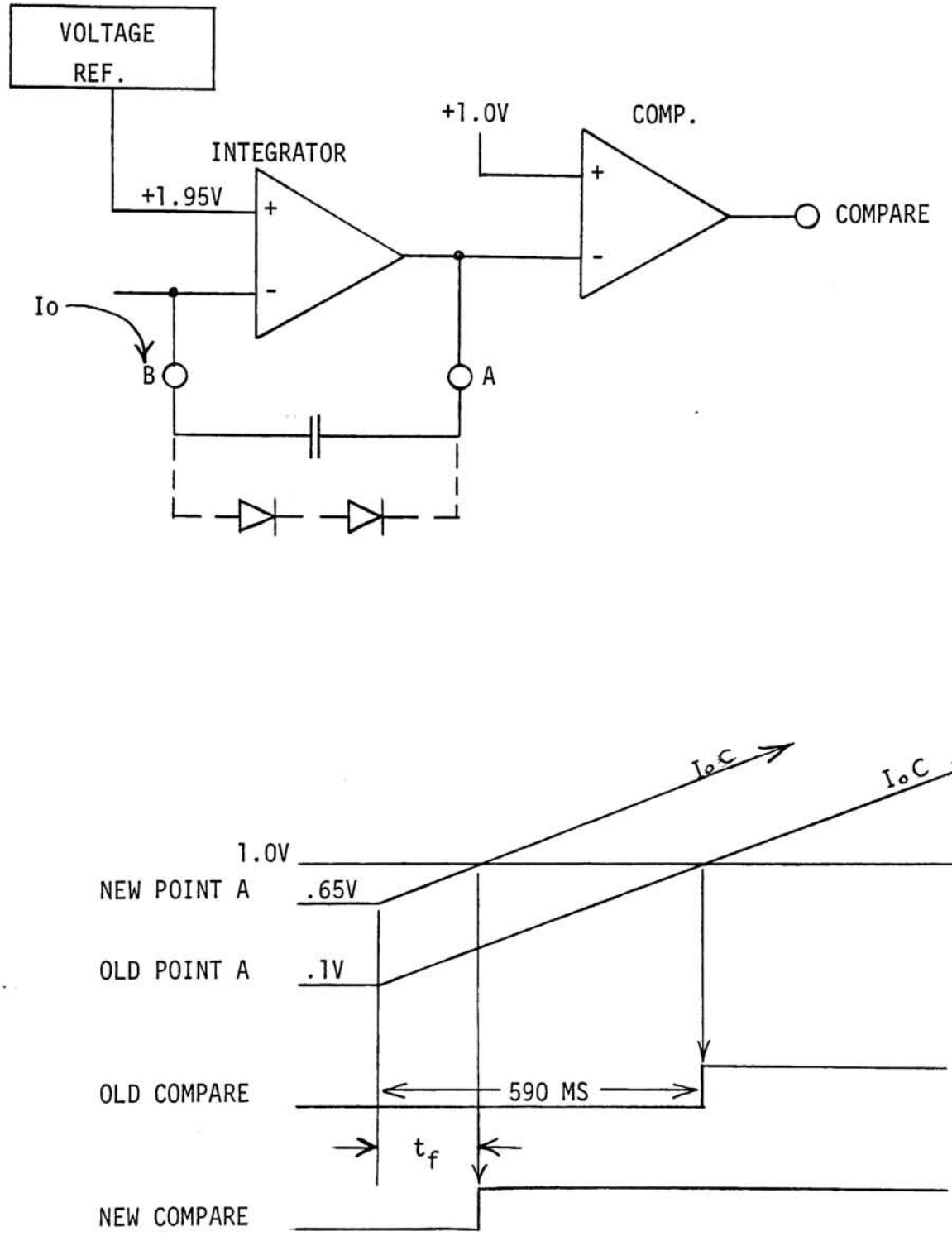


FIGURE 5.25 A/D COMPARE TIMING

The A/D converter was made more accurate by using the simple clock circuit shown in Figure 5.20, location V4-3. The 74132 is a quad 2-input positive-nand schmitt trigger. The 1.1K ohm resistor and 100 picofarad capacitor are the oscillator components. The advantage of this oscillator over other oscillators is that the first period of oscillation is constant. Other oscillators typically use a crystal oscillator-counter combination and use the counter output, such as the last stage of a ÷ 8 counter, as the A/D converter clock. Since the crystal oscillator is asynchronous to the compare signal, the first clock to the counter can occur from zero time to one full oscillator period after the compare signal goes true. With a ÷ 8 counter this represents a first-period error of ± 6.25 percent.

The first oscillation period of the schmitt trigger oscillator is longer than the succeeding periods because the capacitor is initially charged to the voltage at V4-3, or about 4.0 VDC, thereby requiring more time to discharge to the lower hysteresis level. When the lower hysteresis level is reached, the schmitt trigger output switches to 4.0 VDC (nominal) and the capacitor begins charging to that voltage. When the capacitor charges to the upper hysteresis level of 1.7 VDC (nominal) the output switches to the low level. From this time on, the capacitor begins discharging from the 1.7 VDC level, requiring a shorter discharge time than from the initial 4.0 VDC level. Since the first long period exists at the beginning of each conversion cycle, and is constant, the total integration period is always a fixed period of time.

5.4.5 Obtaining the Binary Data Value

The binary data value of the A/D converter is obtained simply by the addition of the fast 74LS197 4-stage binary counter and

the CMOS 4024 7-stage binary counter. The counters obtain the required clock from gate V4-6, which was described in para. 5.4.3, page 130. The timing of gate V4-6 is shown in Figure 5.24, page 137. Two 4512 multiplexers are required to obtain the serial output: "(P) DATA A", which is required for the data compression logic.

5.4.6 Underrange and Overrange Indication

One problem that exists with the dual slope A/D converter is if zero volts is converted and 99 counts are obtained during the down-slope, the BCD counter terminates with a count of 99! When this happens, flip-flop V5-9 (Fig. 5.20) doesn't become set. This flip-flop gets set when the BCD counter reaches 1ØØ (actual count is ØØØØ) during the down-slope count. When count 100 is not reached, flip-flop output V5-8 inhibits both BCD multiplexers with a high voltage level at pin 10, which causes the multiplexed output to read a data conversion value of zero. The switch in location U5-8 is open during A/D calibration so that the 99-ØØ count could be found during the zero adjust with potentiometer W3.

The overrange condition is detected when 1.999 is printed on the line printer. If the BCD counter exceeds 1999, then counter output U4-11 and 12 are high, causing the output of gate R4-13 to go low. When this low level is present at pin 1 of the 74C157 quad 2-input multiplexer, its output is forced to a BCD 9. Output R4-13 also goes to the C/L (count/load) pin of both BCD counters at locations V6 and V7, causing a BCD 9 to load into each counter. The A/D converter BCD counter is then 1999 at the BCD multiplexer whenever the real count exceeds 1998. The switch in location U5-7 is open during A/D calibration so that the 1999-1000 count could be found during the full scale adjustment of potentiometer X3. The +1.9995 VDC

reference voltage on channel 23 is used during full scale calibration.

5.4.7 Obtaining the ΔA Value

The ΔA value is the product of the channel data value and the data tolerance. This value is used by the data compression logic to determine if a data channel has exceeded its tolerance limits.

A design approach using a BCD rate multiplier was selected in paragraph 3.2.1, page 21. The detailed design solution is shown in Figure 5.2, page 95. The two 4167 synchronous decode rate multipliers in locations S7 and S8 obtain the binary-to-BCD converted data tolerance from the data tolerance memory in locations H8 and H9.

The "(P) A/D CNT" to the 74167's is shown at the bottom left corner of Figure 5.2, and originates in Figure 5.20, location V8-6. This clock train provides a string of pulses during A/D conversion which is equal to the multiplexed analog value. The output S7-6 (Fig. 5.2) produces a pulse train consisting of a number of pulses which is equal to ΔA, or the product of the pulses at "(P) A/D CNT" and the data channel tolerance.

The pulses from S7-6 are used to increment an 11-stage binary counter which consists of a fast 74LS197 4-stage binary counter and the CMOS 4024 7-stage binary counter. The ΔA value is multiplexed to the data compression logic with two 4512 multiplexers.

Notice that the LSB of the ΔA value is obtained from gate K4-11 instead of from the LSB of the ΔA counter. The flip-flop in location T4-6 (above the ΔA counter), and associated circuitry satisfy the requirement of assuring that $\Delta A \geq 1$. The T4 F/F

is set at the beginning of a data channel selection at time 4TØ·5T8 from gate J5-4, causing the LSB of the multiplexer input (R6-1) to equal one. If the binary counter is not incremented at least once during conversion then $\Delta A = 1$. The first time the counter is incremented the LSB of the counter (S6-5) goes high, resetting the T4 F/F. This high also goes to NOR gate K4-10, causing the LSB of ΔA at the multiplexer to remain high. From this time on, the multiplexed LSB is equal to the counter LSB. A more detailed description of this circuit is given in para. 5.3.3, page 108.

5.5 Line Printer Sub-System

The complete design of the line printer sub-system is shown in Figure 5.26. This system has been defined and selected in para. 3.2.8, page 74.

The line printer register is shown in the top of Figure 5.26, in location D3 and C2. The "(P) SHIFT-16" shift control is derived from the Data Compression Sub-System (Fig. 5.16), and serially shifts analog, digital, or time data into the print register via AND gates E5-3, E5-4, and E5-10 respectively. All data is in BCD form. The four 4-bit shift registers are labeled digit "A" thru "D". Shift register A contains the LSD and D contains the MSD (1000), the "+" and "-" bits as shown.

Digits A, B, and C are routed to the eight 8-bit multiplexers (type 4512) as shown in Figure 5.26. The decimal point (DP) is also tied to the multiplexers and includes bits E1 thru E4. If the MSD, which originates in location D3-10 (labeled A7) is true then E2 and E4 will be a logic Ø, resulting in an ASCII "$". When A7 is a logic Ø then an ASCII "." will be generated. This will be fully described later.

Each data channel (and time) requires the transmission of 6 ASCII characters. Each character must be transmitted in parallel with an accompanying clock. Figure 5.26 shows the ASCII output, labeled (P)IN01 thru (P)IN06, and the required clock, labeled (P)PICLK. The 6 clock timing pulses are generated from the (P) SHIFT 6Ø2 as shown. The timing for selection and transmission of the 6 ASCII characters is derived from the data compression timing (see Figure 5.15 and 5.16) and includes (P)Ø1, (P) SHIFT 6Ø2, and (P) CNT-G. Figure 5.27 shows how these signals are used to obtain the 6 character selection, using the 4017 decimal counter/decoder.

The first (P) SHIFT 6Ø2 pulse sets the Count En. F/F (location G6, G7) enabling the (P) Ø1 count pulses to pass thru gate E4-E and to the 4017 counter. The first (P) SHIFT 6Ø2 pulse is also used as the first (P) PICLK strobe during count Ø. Note that during count Ø and 1 the counter outputs, pins 3 and 2, force the output of NOR

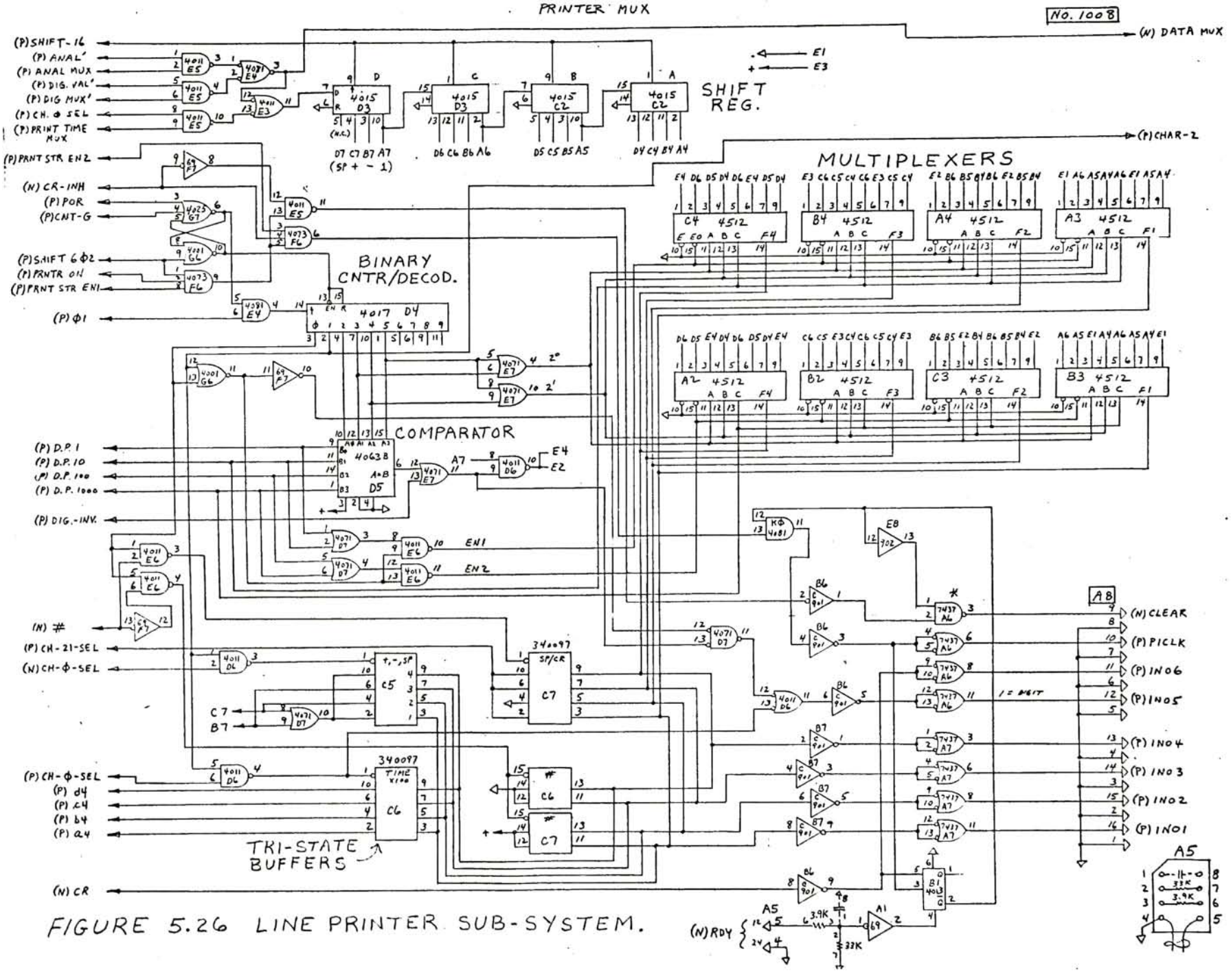


FIGURE 5.26 LINE PRINTER SUB-SYSTEM.

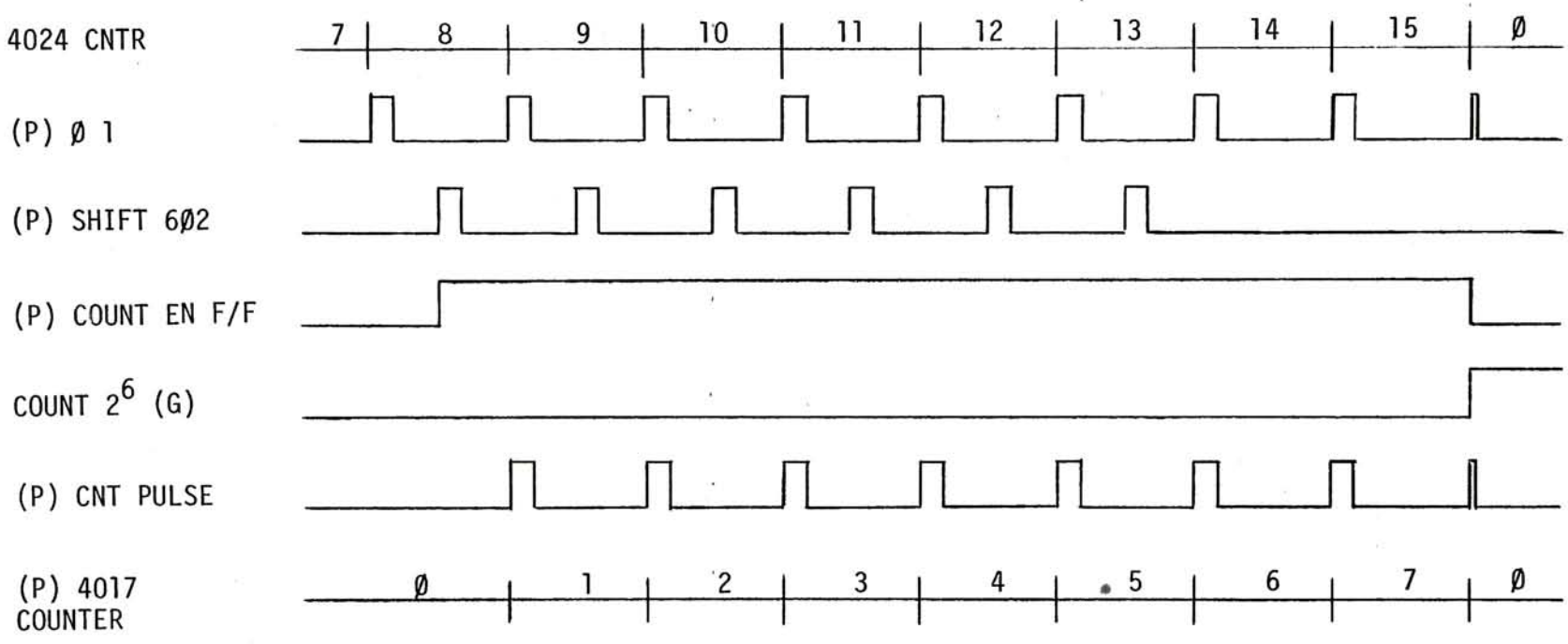


FIGURE 5.27 ASCII CHARACTER TIMING

gate G6-11 to a logic Ø, inhibiting multiplexer enable gates E6-10 and 11 and causing (P) IN05 to be a logic Ø. If "(N)#" is low during count Ø, gate E6-4 goes low, enabling the "#" code ØØ11 to be transmitted to (P) IN04 thru (P) IN01 respectively the (N) CR signal is high, resulting in (P) IN06 = 1. The ASCII code is then Ø1ØØØ11, which is an ASCII "#". Note that the ASCII codes in Table 3.2 always require BIT 7 to be Ø for all the circled characters which are used by the printer. Also note that BIT 6 is Ø only for the "CR" code, and that only the (N) CR signal controls BIT 6. Further, note that BIT 5 [or (P) IN05] is a 1 for digit codes only.

If "(N) #" is high during count Ø then E6-3 goes low, selecting the lower 4 bits of the SPACE code.

During count 1 gates D6-3 and D6-4 are enabled and select the multiplexers in locations C5 and C6 respectively. If (P) CH-Ø-SEL is true, then multiplexer C6 is selected, enabling the seconds X100 digit to be transmitted as the second ASCII character (see Table 3.3, column 2). If (N)CH-Ø-SEL is false (high), then multiplexer C5 is selected, enabling the lower 4 ASCII bits of the "+" or "-" code to be transmitted. Note that signal C7 and B7 originate from the printer register, locations D3-4 and D3-3 respectively, and represent the "+" and "-" values respectively.

During counts 2 thru 5 the four top multiplexers are selected with gate E6-10 when (P) D.P.1 or (P) D.P.10 are selected, and the "C" input select is 1 when (P) D.P.10 is true, or Ø when (P) D.P.1 is true. The bottom 4 multiplexers are selected in the same manner, using (P) D.P.100 and (P) D.P.1000.

The select A and B inputs are controlled by encoding counts 2 thru 5 of the 4017 counter with the two OR gates in location E7-4 and 10. For counts 2 thru 5 these gates select A and B of all eight multiplexers in a binary ØØ, Ø1, 1Ø, 11 sequence as shown in Table 5.3-(a). This table also shows how select C and the top and bottom rows of multiplexers are selected by the (P) D.P. signals.

The result of this multiplexing scheme is that the four combinations of the three data digits and decimal points can be selected by the four (P) D.P. signals. Table 5.3-(b) shows the sequence in which the data digits (C,B,A) and the D.P. or "$" is transmitted during counts 2 thru 5 respectively. Note that signal A7 determines whether a D.P. or a "$" code is to be transmitted. Signal A7 accomplishes this by controlling bits E2 and E4 with the NAND gate in Figure 5.26, location D6-10. Bits E1 and E3 are always low and high respectively.

The RCA type 4063B 4-bit magnitude comparator is required to change (P) IN05 to a logic Ø when the D.P. or "$" is to be transmitted. This is accomplished by comparing the four (P) D.P. signals with the decoded 2 thru 5 counts of the 4017 decode counter/decoder. When a compare is made, D5 pin 6 goes high and forces (P) IN05 low thru gates E7-11, D7-11, D6-11, B6-5 and A6-11.

If the printer buffer contents are to be printed, a CR code is transmitted during selection of channel 21. This is accomplished by making (P)CH-21-SEL and (N)# go high and by making (N)CR go low, causing the "SP/CR" multiplexer in location C7 to become selected and to transmit the lower 4 bits of the CR code. (N)CR forces (P)IN06 (BIT 6) to go low. The (N)CR-INH signal goes high to enable a (P)PICLK pulse during count Ø. Count 1 produces signal (P)CHAR-2 which resets an external F/F, causing the (P)PRNT STR EN1 signal to go low. This signal then inhibits the remaining five (P)PICLK pulses.

If printout of the data buffer contents is not required, the (N)CR-INH signal goes low during the channel 21 select time causing one (N)CLEAR pulse to occur during count Ø. Note that gate F6-9 must also be enabled with signal (P)PRNTR on which is derived from the PRINTER ON/OFF switches on the control panel.

	(P) D.P.1			(P) D.P.10			(P) D.P.100			(P) D.P.1000		
	TOP MUX SELECT						BOTTOM MUX SELECT					
	A	B	C	A	B	C	A	B	C	A	B	C
COUNT 2	Ø	Ø	Ø	Ø	Ø	1	Ø	Ø	Ø	Ø	Ø	1
COUNT 3	1	Ø	Ø	1	Ø	1	1	Ø	Ø	1	Ø	1
COUNT 4	Ø	1	Ø	Ø	1	1	Ø	1	Ø	Ø	1	1
COUNT 5	1	1	Ø	1	1	1	1	1	Ø	1	1	1

TABLE 5.3(a) PRINTER MUS SELECTION CODES

	DATA VALUE	
	A7 = Ø	A7 = 1
(P) D.P.1	.CBA	$CBA
(P) D.P.10	C.BA	C$BA
(P) D.P.100	CB.A	CB$A
(P) D.P.1000	CBA.	CBA$

TABLE 5.3(b) SELECTION OF D.P. AND "$" LOCATION

5.6 Data Channel Input-Interface Control

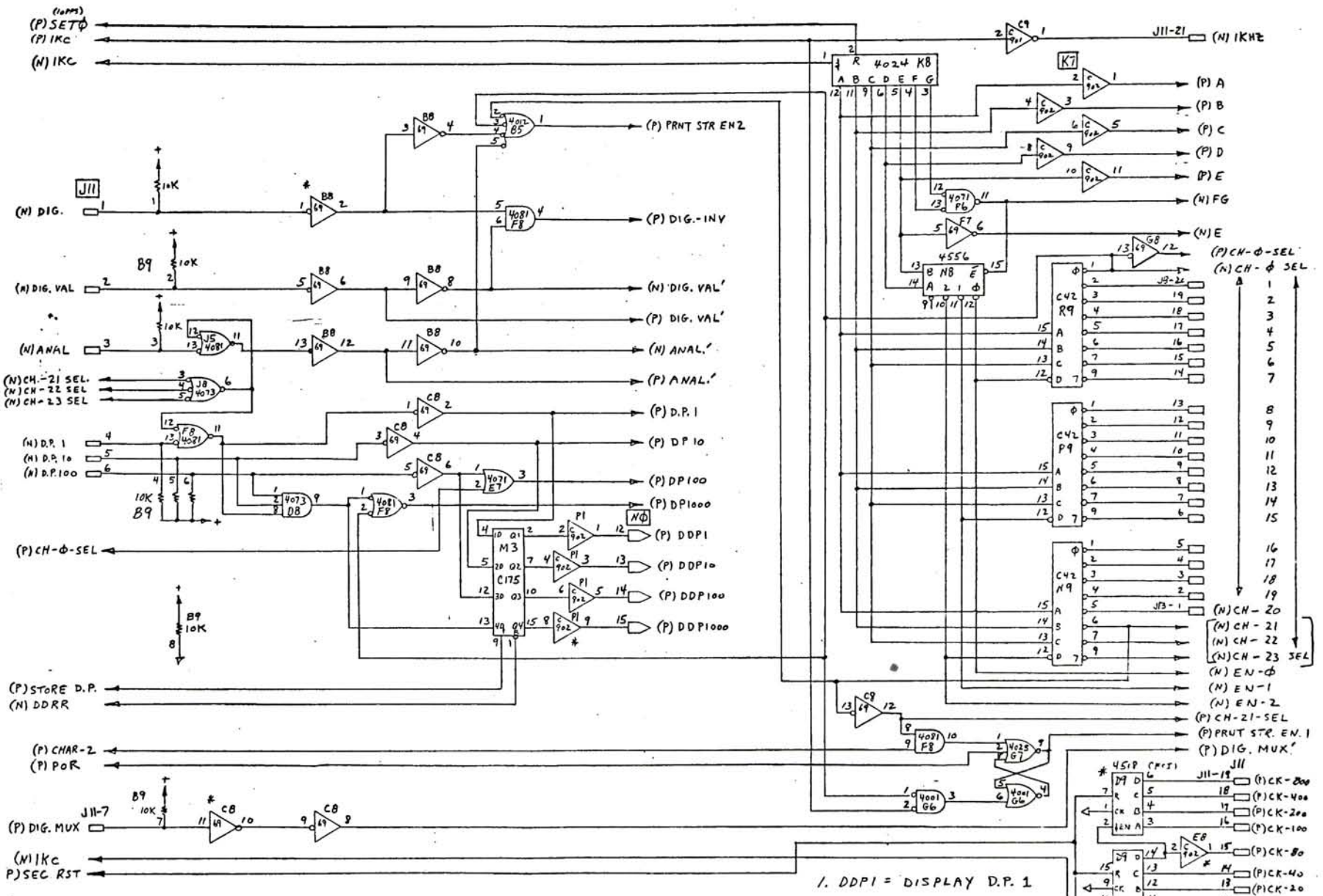
Figure 5.28 shows all the input lines from the data channels as rectangular pins on the left side of the schematic. Gate B5-1 generates a true (P)PRNT STR EN2 output when the (N) DIG., (N)ANAL, (P)CH-Ø-SEL, or (P)CH-21-SEL signals are true, enabling transfer of data to the printer line buffer.

When a digital channel is selected and it has no valid data, (N)DIG. is true and (N)DIG. VAL is false, generating the true (P)DIG.-INV. signal. This signal causes only the D.P. of the selected digital channel to be printed.

Notice how (N)D.P.1, 10, and 100 produce signals (P)D.P.1, 10, 100, and 1000. OR gate F8-11 also produces (P)D.P.1 if (N)CH-21 SEL., (N)CH-22-SEL., or (N)CH-23-SEL. are true.

The (P)DIG. MUX is tied to the serial MUX output of each of the 20 digital channel outputs which are tri-state and wire-or'd. The (N)DIG., and (N)DIG. VAL. signals are also tri-state and wire-or'd. The (N)ANAL and three (N)D.P. signals are all wire-or'd diodes as shown in Figure 3.27.

Note that the quad F/F register in location M3 (Fig. 5.28) is required to store the D.P. information for the control panel data display.



1. DDP1 = DISPLAY D.P. 1

FIGURE 5.28 DATA CHANNEL I/O CONTROL

5.7 Miscellaneous System Functions

The miscellaneous functions are those functions which are not a part of any of the previously discussed sub-systems.

The four data sample rate selection switches on the control panel enable selectable print rates of one line per second, 10 seconds, minute, and 10 minutes. The timing logic for this requirement is shown in the top half of Figure 5.5. The one pulse per second rate is generated by AND gate T2-4. This signal is used as the clock for generation of the remaining three time intervals and is also used to set F/F R2-2 if the one second rate is selected. The remainder of the timing logic is straight-forward and will therefore not be described.

The 7-stage binary counter shown in Figure 5.28 performs a number of selection functions. It is shown controlling three 74C42 decade counter/decoders which in turn are used to select channels Ø thru 23. The 4556 decoder outputs select the three 74C42's and also selects the analog multiplexers for the A/D converter sub-system (Fig. 5.20, locations X7, 8, and 9). Outputs (P)A thru (P)E (Fig. 5.28) also select the analog multiplexers, the data tolerance memory (Fig. 5.2, location H8), the data compression memory (Fig. 5.16, location P7), and all digital multiplexers.

Figure 5.29 includes the real-time clock shown in locations DØ and D1. This clock counts from ØØØ.Ø to 599.9 seconds. Notice that the (P)DISP. TIME MUX multiplexes XXX. seconds and the (P)PRINT TIME MUX multiplexes XXX.X seconds.

The system power-on-reset (POR) is generated by the circuit in the lower right corner of Figure 5.29. All on-board voltage regulation is shown in the lower left corner of Figure 5.29.

The remainder of Figure 5.29 includes the control panel interface logic for the switch inputs which are shown as circled input pins.

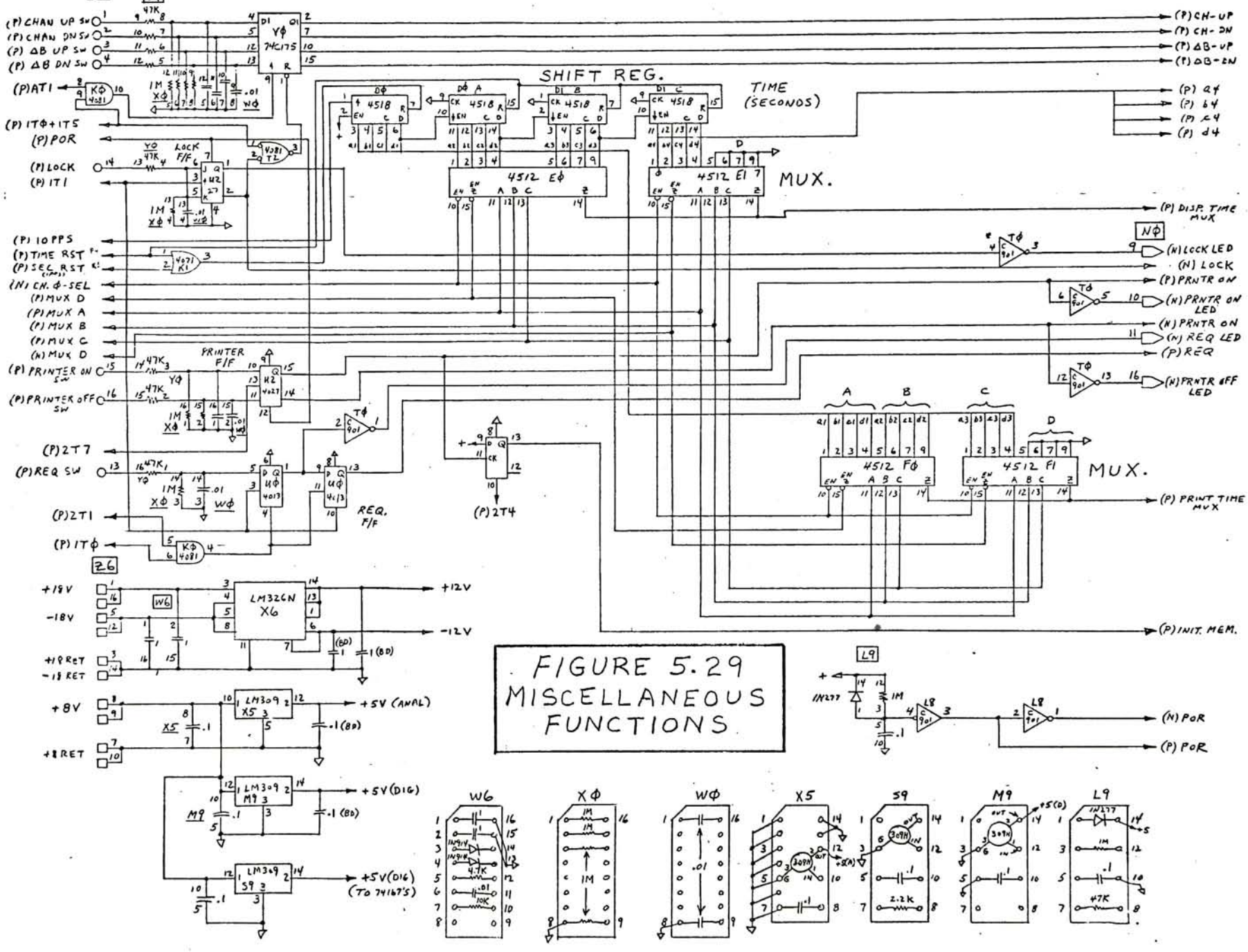


FIGURE 5.29
MISCELLANEOUS FUNCTIONS

6. Results

The S.D.C.S. was built and debugged. The calibration procedure for the A/D Sub-System was as follows: Channel 21 was selected on the Control Panel Monitor. This channel selection applies analog ground to the VOLTAGE FOLLOWER (see Figures 5.18 and 5.20). The 10K ohm offset-adjust potentiometer in the VOLTAGE FOLLOWER circuit was adjusted to obtain an output of 0.000 VDC. The 10K ohm offset potentiometer on the bottom 1319 (Philbrick) operational amplifier in the ABSOLUTE VALUE CIRCUIT (see Figures 5.19 and 5.20) was then adjusted to obtain 0.000 VDC at the input to the A/D converter. Before this adjustment was made, the offset potentiometer on the top 1319 circuit had to be adjusted to obtain a negative voltage at the output of that 1319. This enabled the bottom 1319 to drive the output of the ABSOLUTE VALUE CIRCUIT to 0.000 VDC.

The next step involved adjustment of the -1.000 VDC and +2.000 VDC references shown in Figure 5.18 and 5.20. A 4-1/2 digit digital voltmeter was required for adjustment of both reference voltages and for all other voltage adjustments. The -1.000 VDC reference was then multiplexed to the VOLTAGE FOLLOWER by selecting channel 22. The offset potentiometer of the top 1319 circuit in the ABSOLUTE VALUE CIRCUIT was then adjusted to obtain +1.000 VDC at the A/D converter input.

Channel 21 was then selected to apply zero volts to the A/D Converter. The ZERO ADJ. potentiometer was then adjusted to obtain +0.000 VDC on the S.D.C.S. data display. Channel 23 was then selected to switch the +2.000 VDC reference to the A/D Converter. The FULL SCALE ADJ. potentiometer was adjusted to obtain +1.999 VDC on the S.D.C.S. data display. Because these two adjustments are interactive, it was necessary to make repeated adjustments to obtain proper calibration of the A/D Converter.

Please note that the actual reference voltages were adjusted for -.9995 VDC and +1.9995 VDC, but that I chose to refer to them as -1.000 VDC and +2.000 VDC respectively.

The next step involved a check on the linearity of the A/D Converter Sub-System. This was accomplished by applying the output of a variable voltage reference power supply to one of the analog input channels and monitoring the selected channel on the control panel while varying the voltage from 0.000 VDC to +1.9995 VDC in increments of .100 VDC. The maximum deviation of the A/D Converter was one count over the full range. The test was repeated for an input of 0.000 VDC to -1.9995 VDC with the same maximum error of one count. The average error for the full range was -.098 counts.

All 20 analog multiplexer inputs were checked by applying a +1.000 VDC input and checking the DATA DISPLAY on the S.D.C.S. Control Panel for a readout of +1.000 VDC.

The multiplexed digital data channel input to the S.D.C.S. system was checked for proper operation by building the "CHANNEL X" circuit shown in Figure 3.25, page 68. An 8-switch dual-in-line unit was tied to each 4512 circuit, with the common of each switch tied to ground. The switches were set to read 1999 in BCD format, and the (N) DP-1, (N) DIGITAL, and (N) DIGITAL VALID signals (see Figure 3.26, page 70) were tied to ground. The The print rate of one line per second was selected and the printer was turned on. The printer printed time and the number "$999" every second, with the time printout of 000.0, 001.0, 002.0, etc. The digital channel was monitored to verify the DATA DISPLAY of 1.999. Other values were selected with the switches and verified on the printer and digital readout.

The (N) DP-10 and (N) DP-100 signals were sequentially grounded to obtain printouts of 9$99 and 99$9 respectively. With all three (N) DP signals flouting, a printout of 999$ was obtained.

The Data Compression Sub-System was checked by setting the tolerance for channel 10 to 10 percent, applying a variable voltage reference power supply to channel 10, setting the data compression sample rate to 10 samples per second, and selecting the print ON mode. When the print ON mode was initiated, the printer immediately printed time and +0.010, which represents

+0.010 VDC (voltage reference value). The (N) DP-1 was selected, and represents a full scale range selection of 1.000 VDC, with an overrange of 1.999 VDC.

The voltage reference supply was then slowly increased to +1.999 VDC. The printout verified that the tolerance selection of 10 percent caused printout each time the voltage reference supply changed by 10 percent from its previous printout value.

The S.D.C.S. was first used to collect data from a test fixture containing optical sensors which were used to detect the leading or trailing edge of a sheet of paper as it moved thru the test fixture. The picture in Figure 6.1 shows the front view of the S.D.C.S. with one dual AC/DC voltmeter module and four identical dual digital modules. Each digital module can measure the time that two sensors activate or deactivate.

Figure 6.2 shows a top view of the S.D.C.S. with the top cover removed.

Figure 6.3 is a top-back view and Figure 6.4 is a back view of the S.D.C.S.

Figure 6.5 shows the S.D.C.S. with the Versatec line printer.

A SYNC. input was added to the control panel of the S.D.C.S. (see Fig. 6.1) to satisfy a request to initialize the real-time clock each time a SYNC pulse occurred.

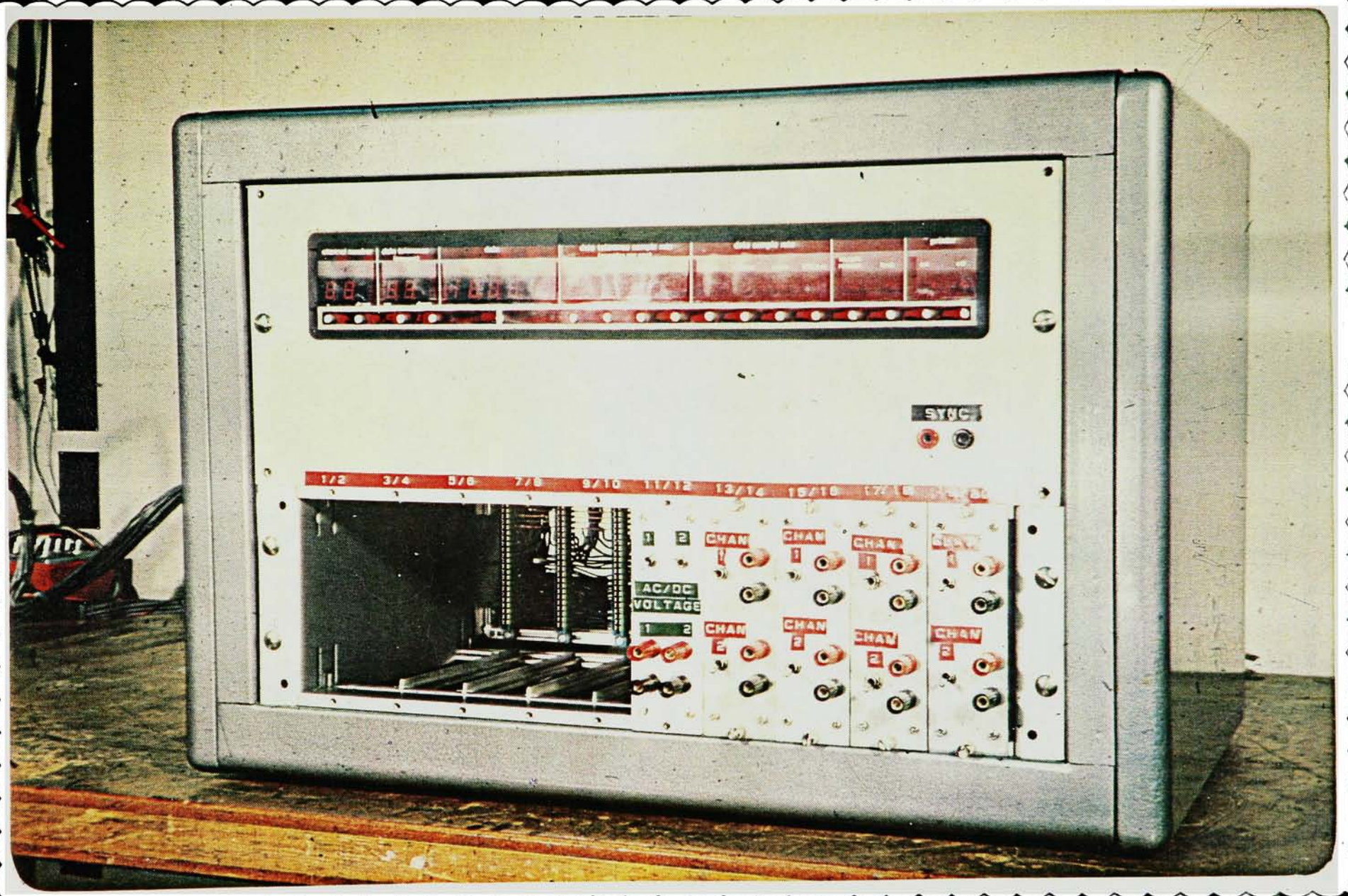


FIGURE 6.1 S.D.C.S., FRONT VIEW

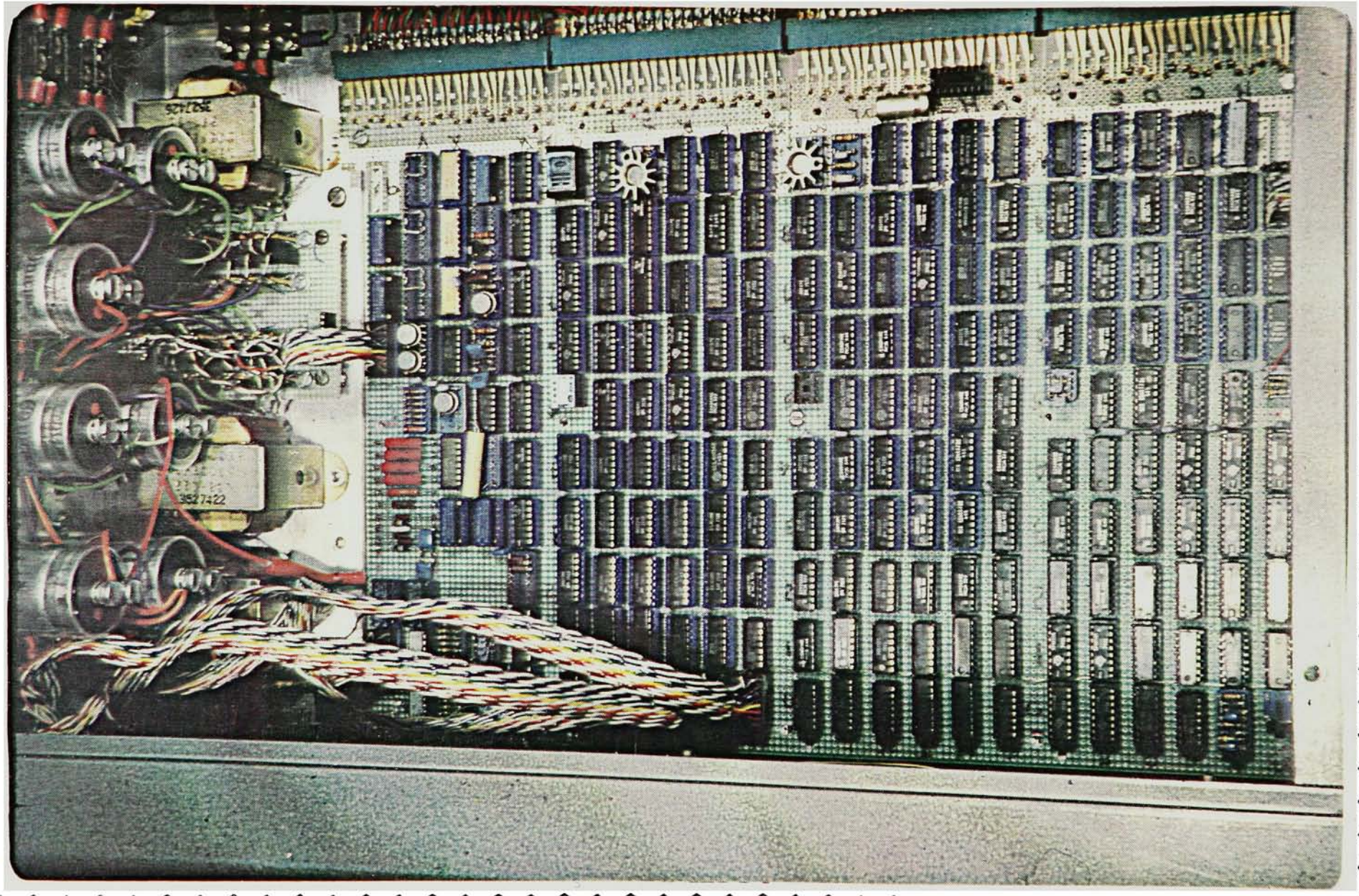


FIGURE 6.2 S.D.C.S., TOP VIEW

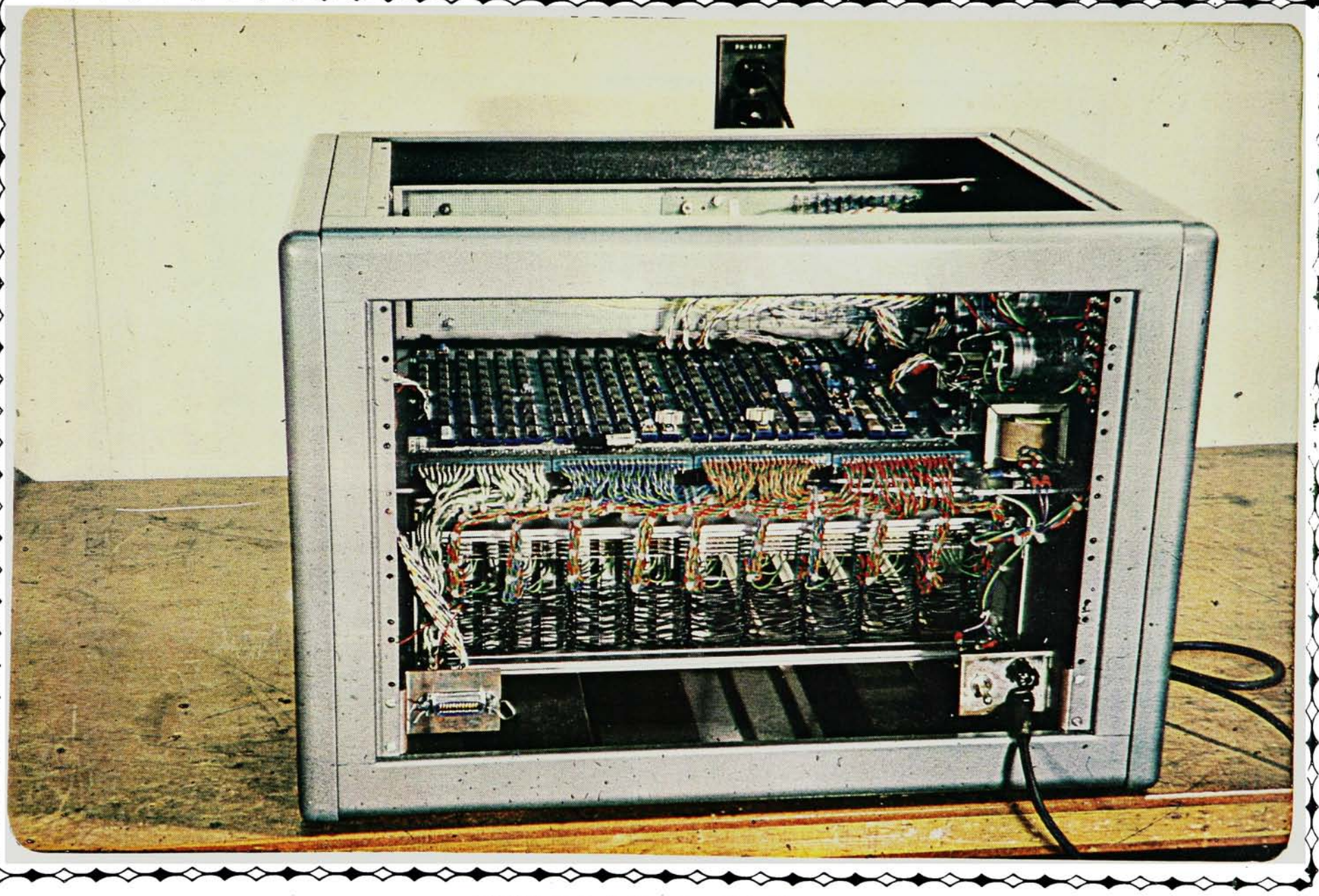


FIGURE 6.3 S.D.C.S., TOP-BACK VIEW

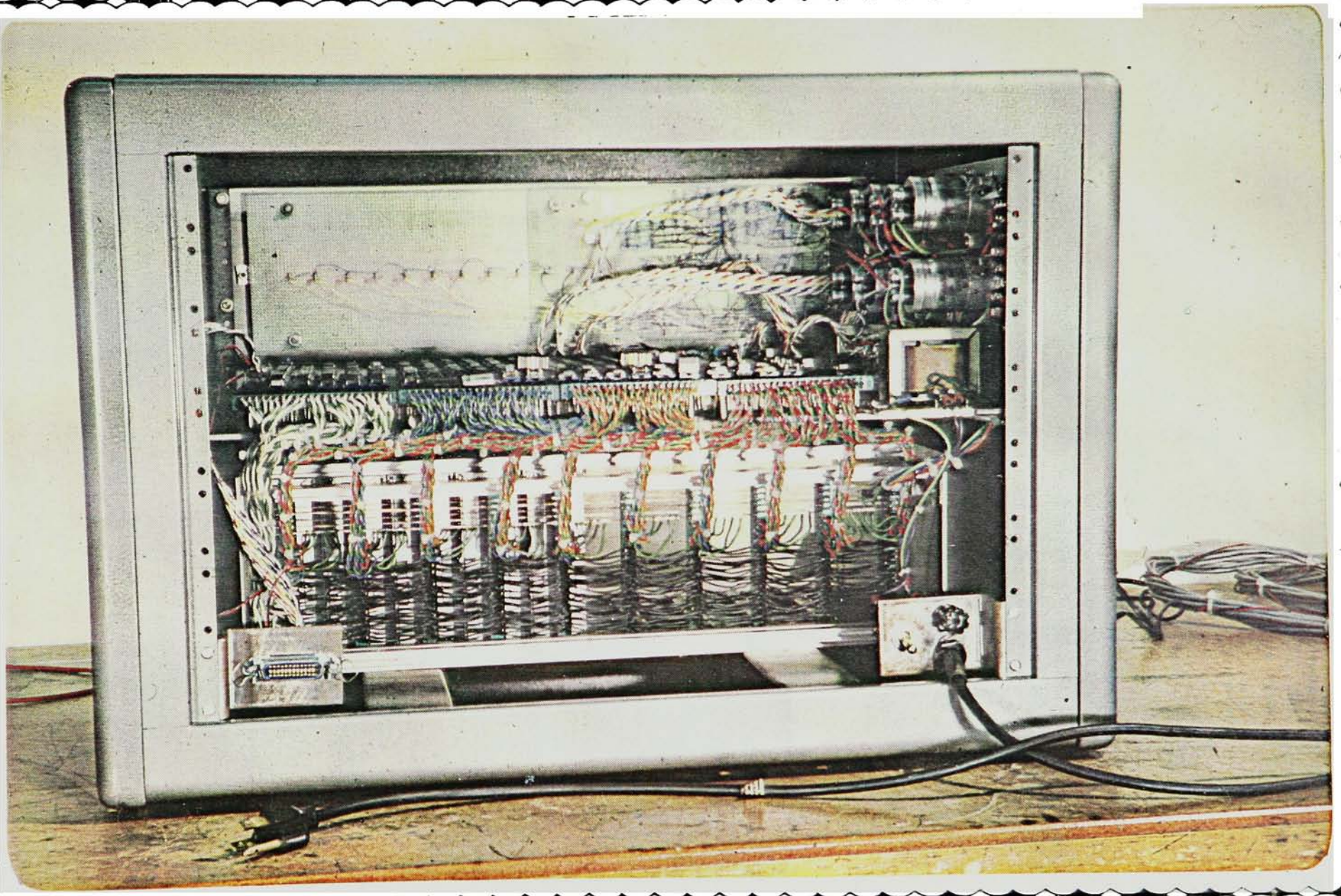


FIGURE 6.4 S.D.C.S., BACK VIEW

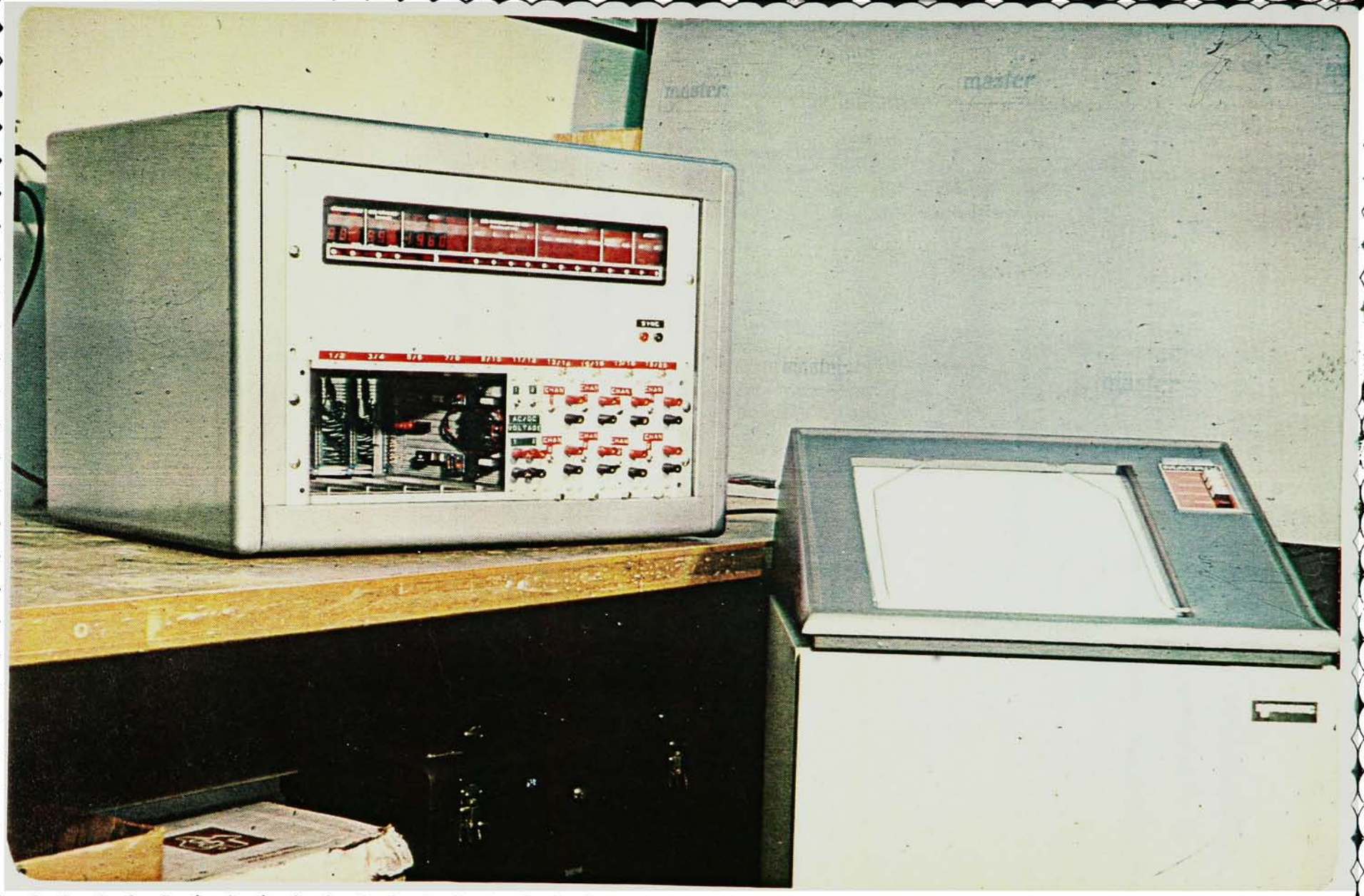


FIGURE 6.5 S.D.C.S., AND LINE PRINTER

The S.D.C.S. is capable of measuring a wide range of analog and digital functions. The following is a partial list of measurements which can be made when the proper transducers are used.

6.2.1 AC/DC current and voltage.

6.2.2 Resistance.

6.2.3 Event time and count.

6.2.4 Pulse width, time of arrival.

6.2.5 Temperature.

6.2.6 Humidity.

6.2.7 Pressure (Dynamic/static/diff.).

6.2.8 Distance, velocity, acceleration.

6.2.9 Air flow.

6.2.10 Torque.

6.2.11 Frequency.

6.2.12 Illumination.

6.2.13 Paper parameters such as skew, shift, count, timing and curl.

7. Summary

This thesis has shown the reader the requirements of a data acquisition system which is necessary to monitor tests conducted on various types of equipment containing analog and digital functions. The data acquisition system requirements were specified and the system was designed, built, and made fully operational. The Top-Down(1) design approach was very effective in the selection and development of the sub-systems of the S.D.C.S.

(1) See Appendix A.

APPENDIX A
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